# UNIVAC<sup>®</sup> Solid-State Computer

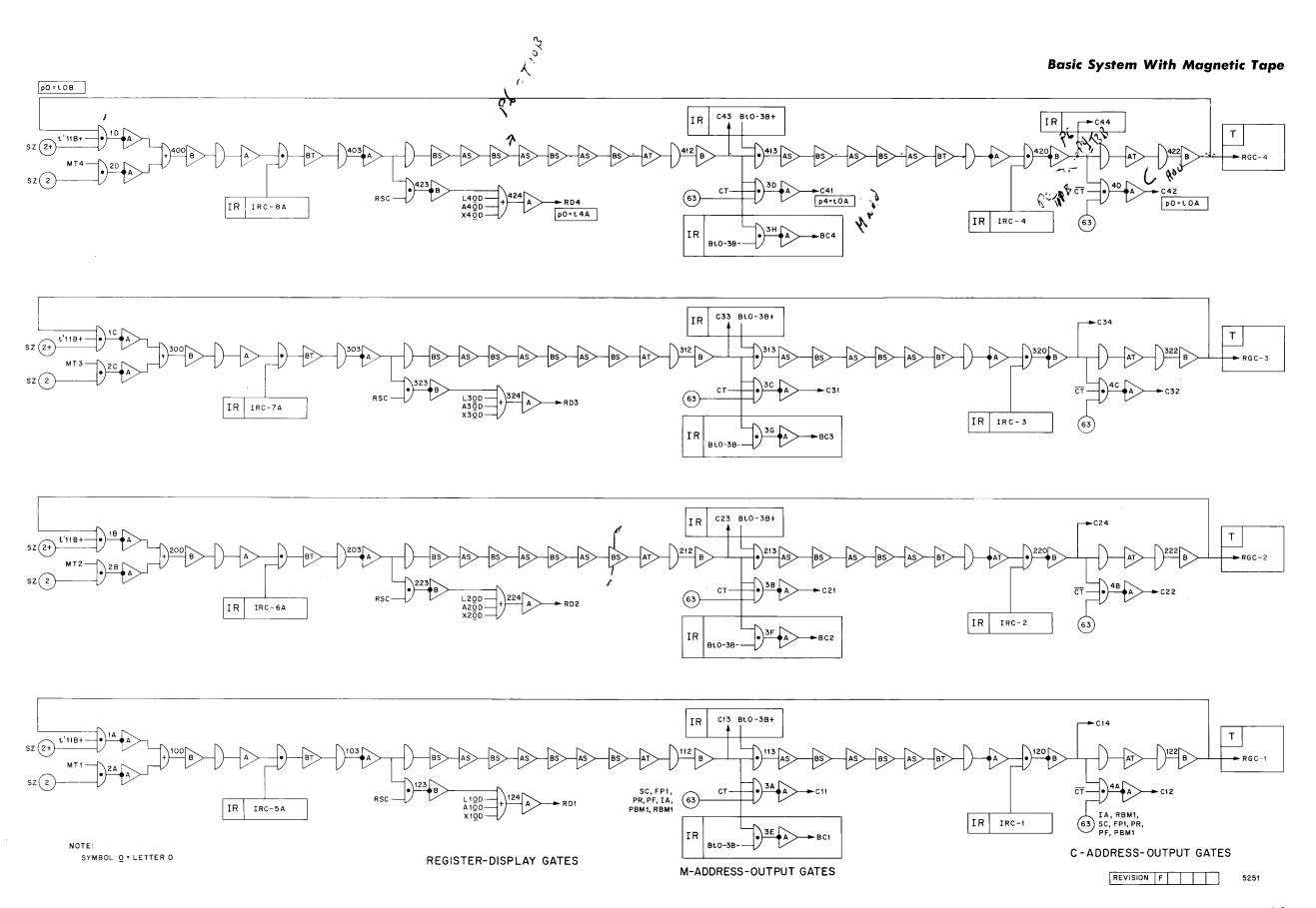
Manual 2 -

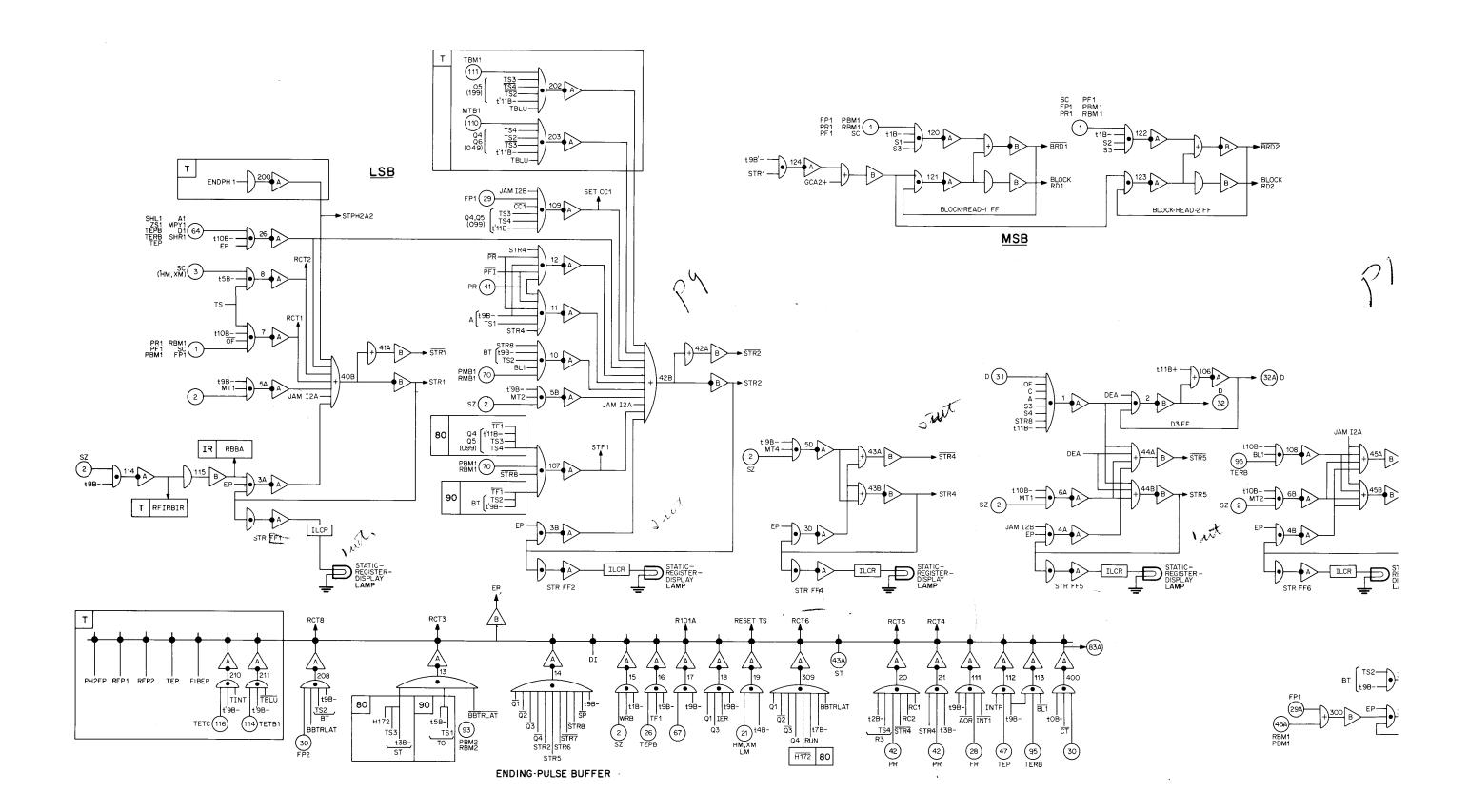


Volume IA

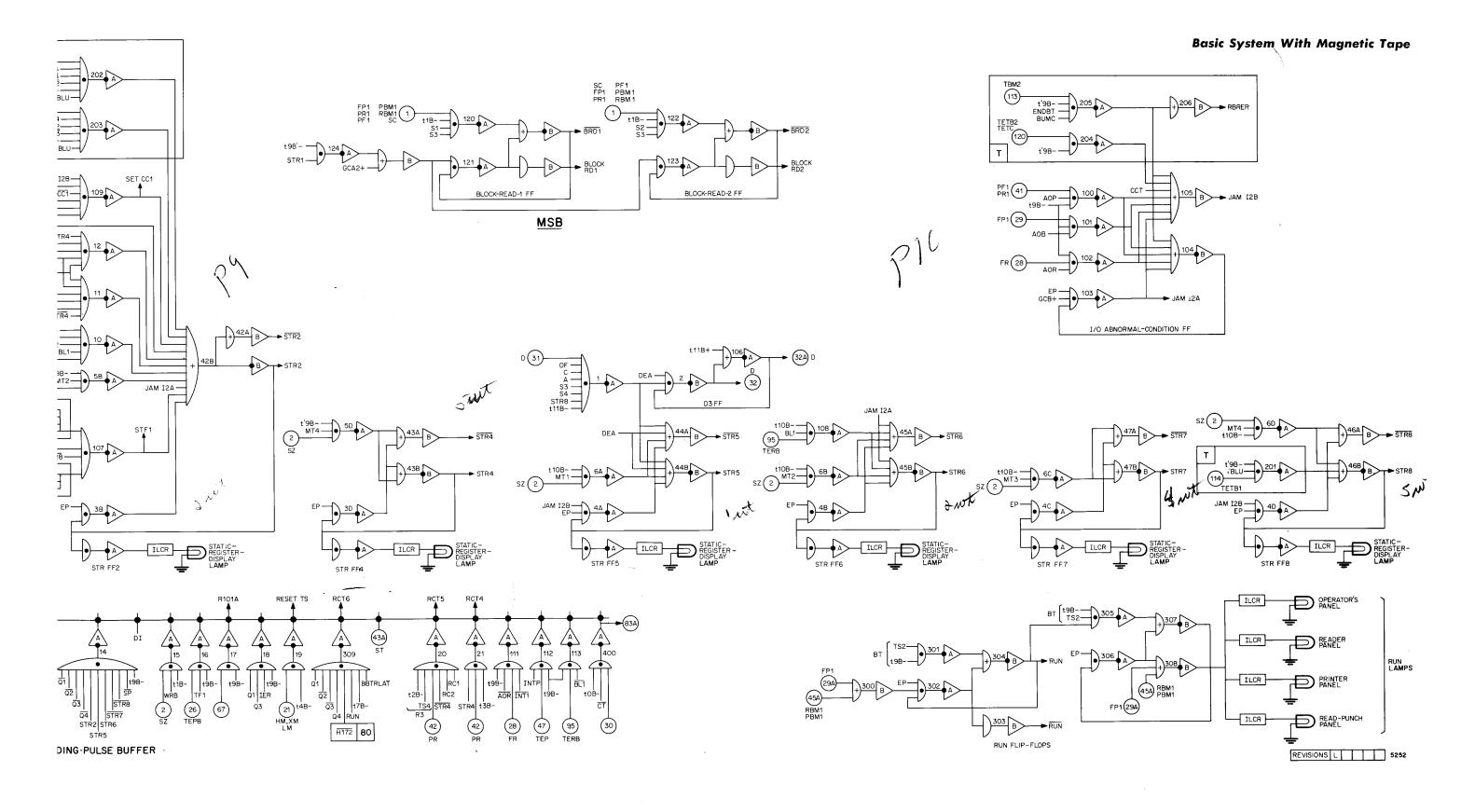
BASIC SYSTEM WITH MAGNETIC TAPE Models 13.0 and 131

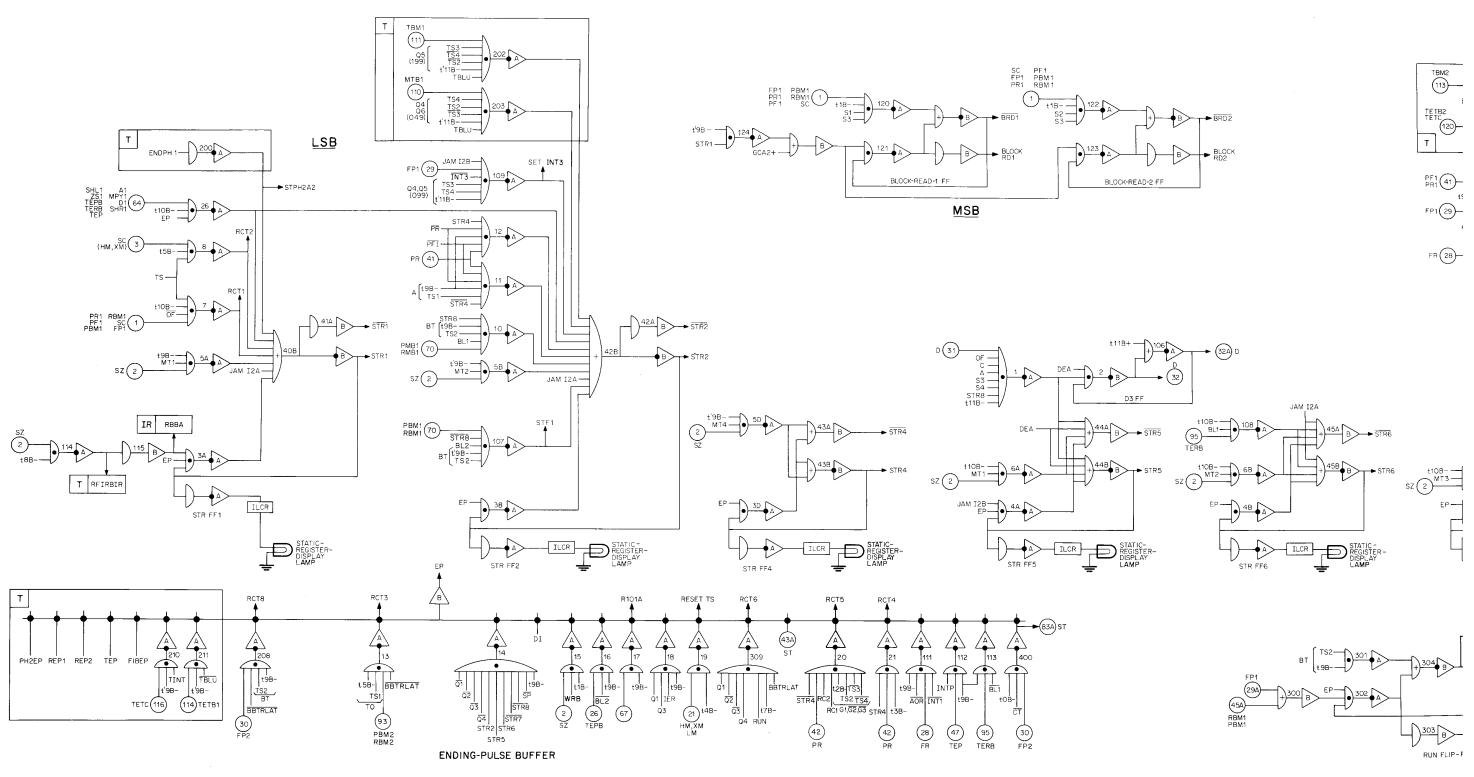
REPLACED BY VOLUME 1B



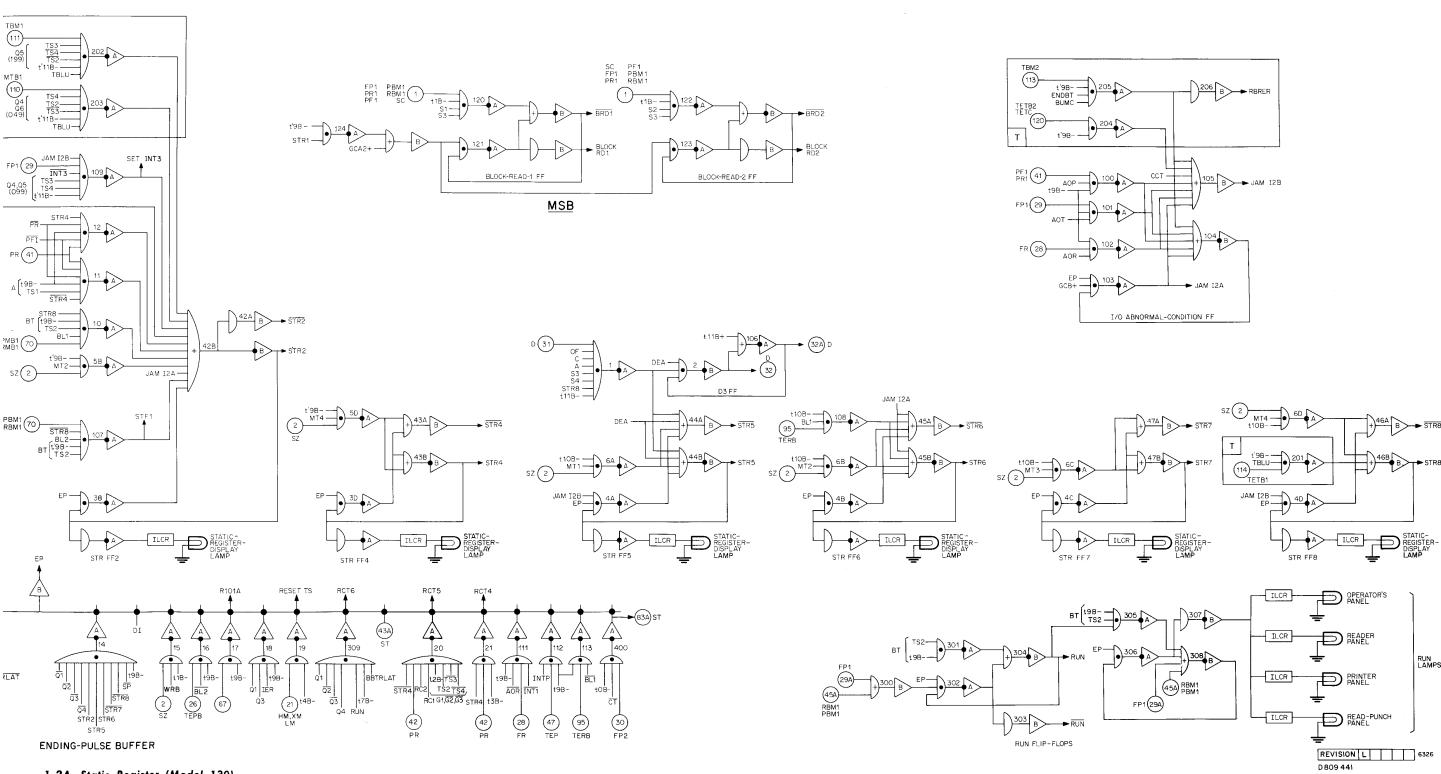


1-2A. Static Register (Model 131)

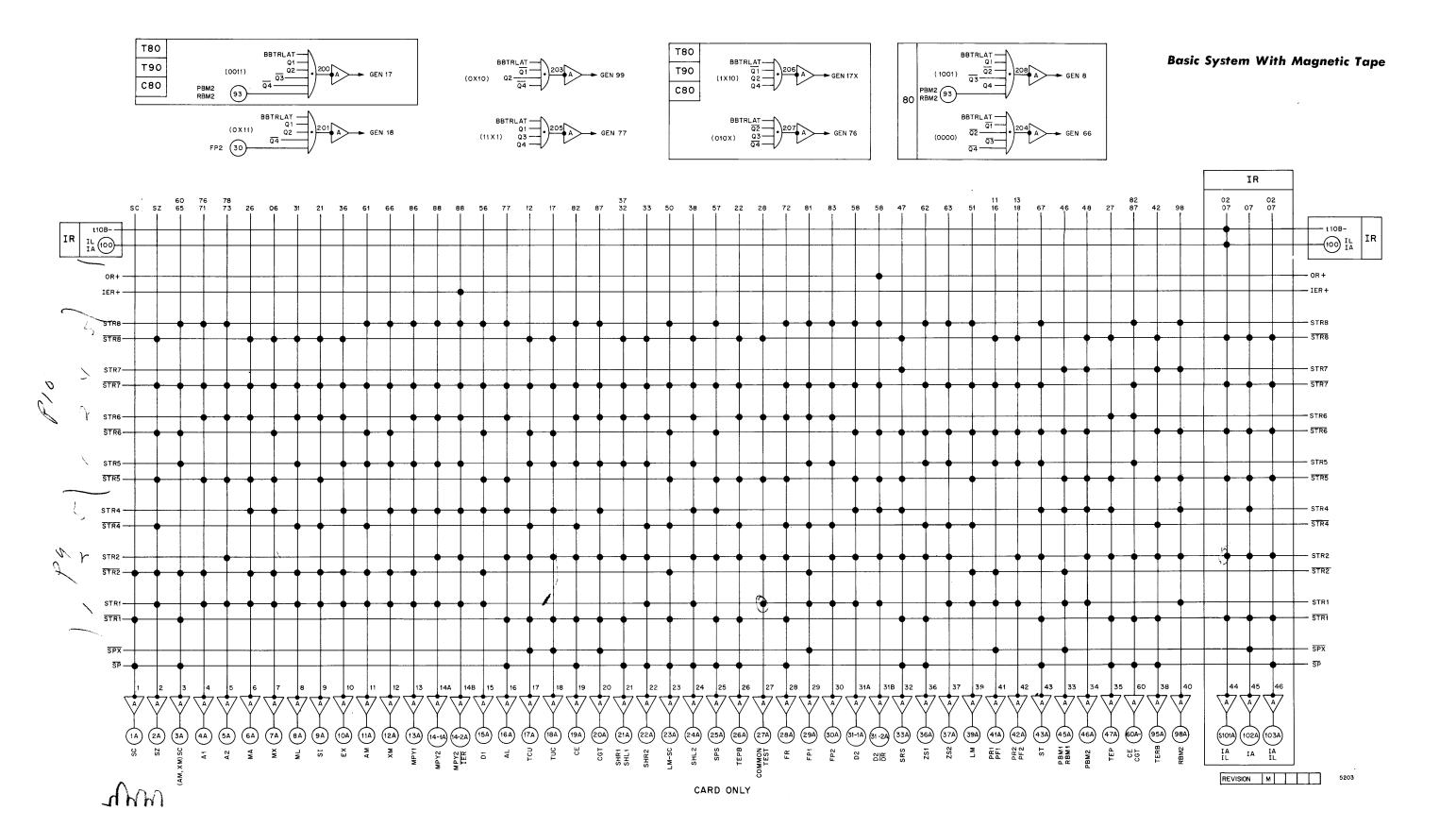


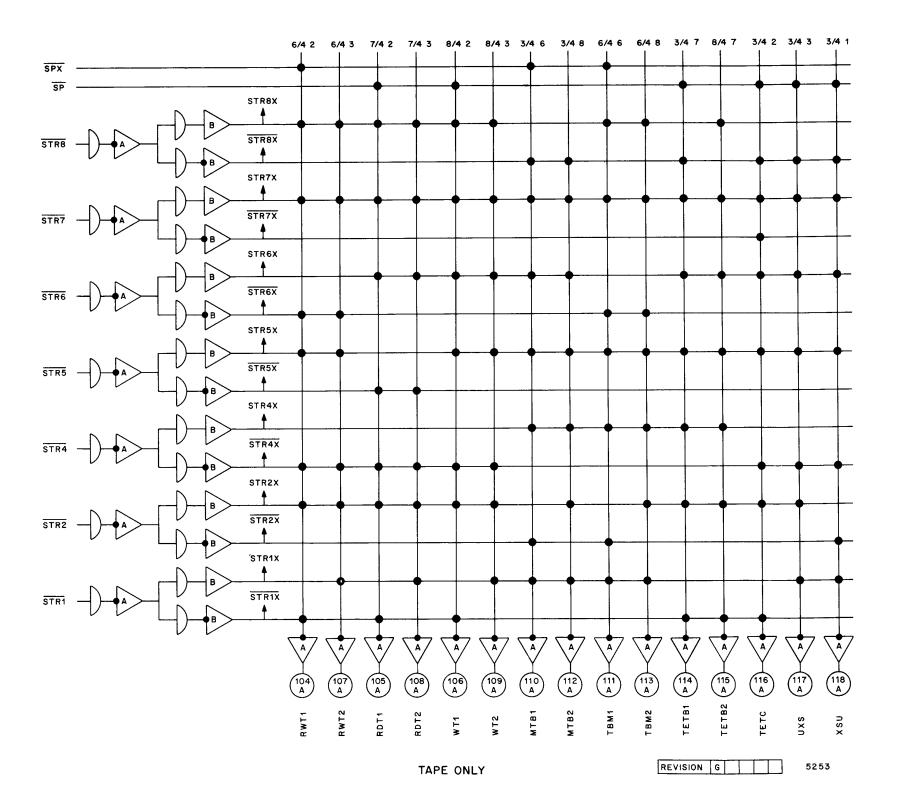


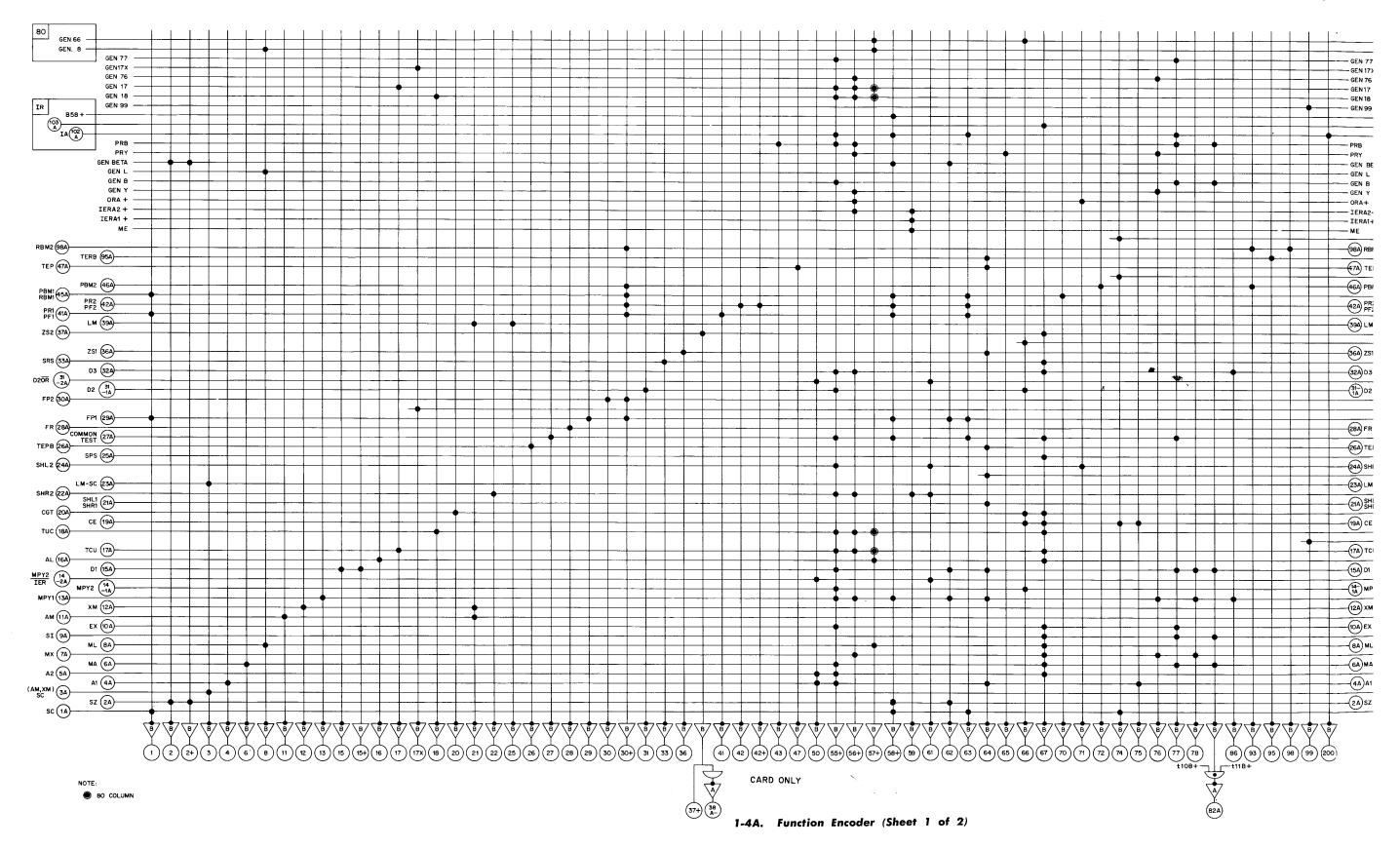
1-2A. Static Register (Model 130)

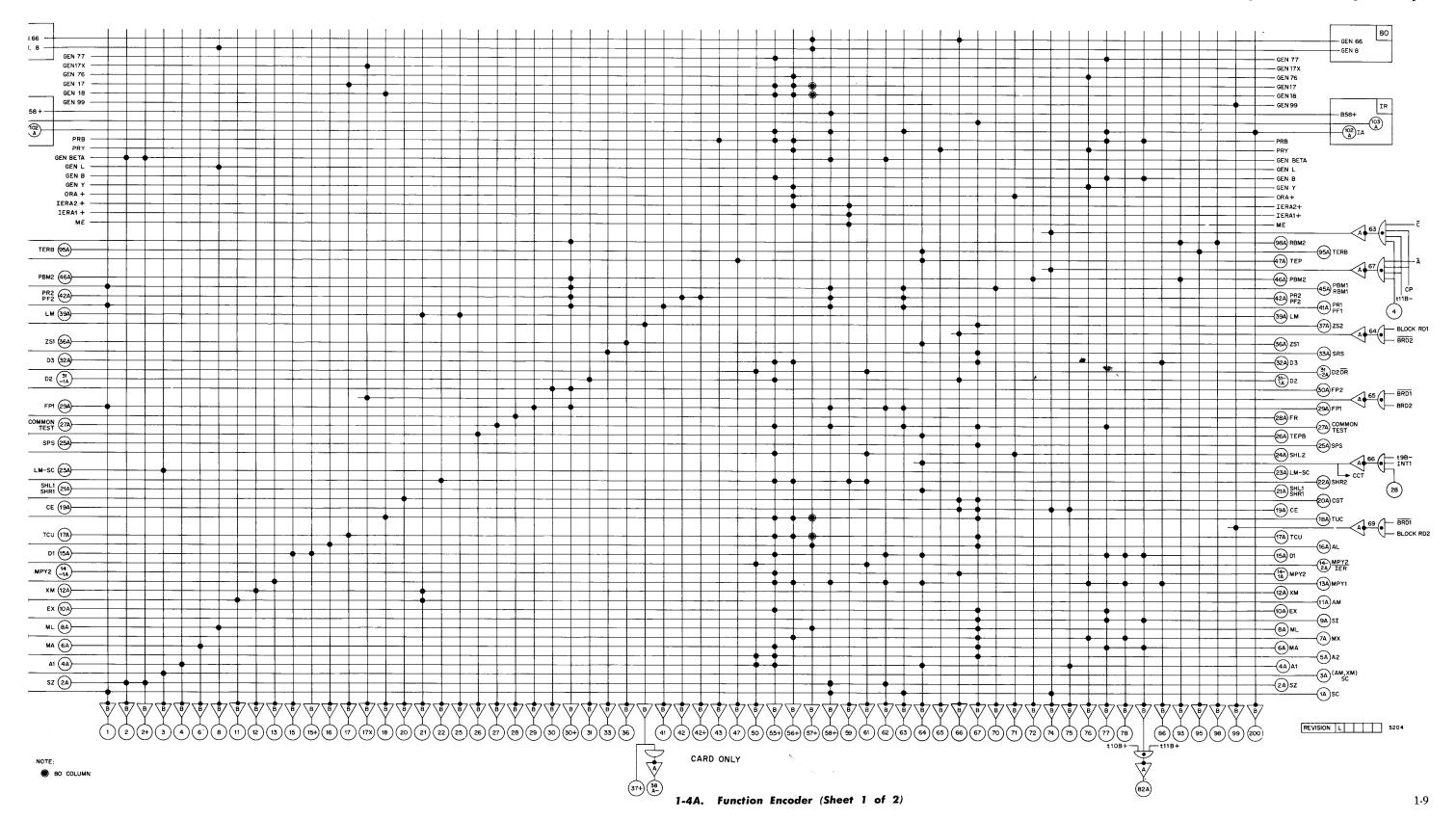


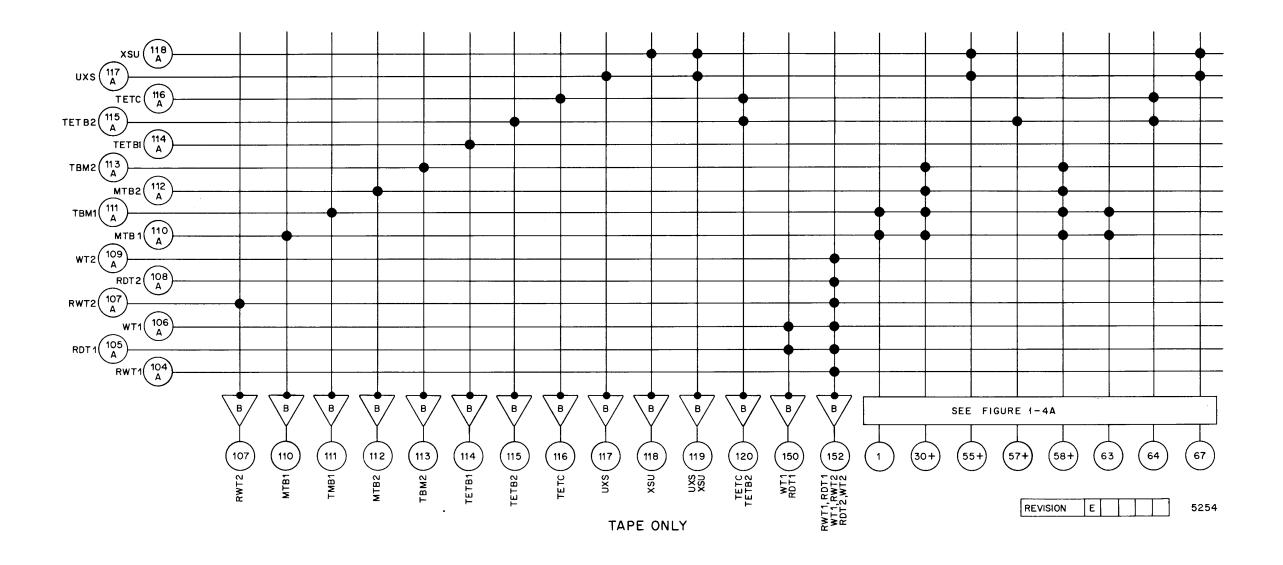
1-2A. Static Register (Model 130)

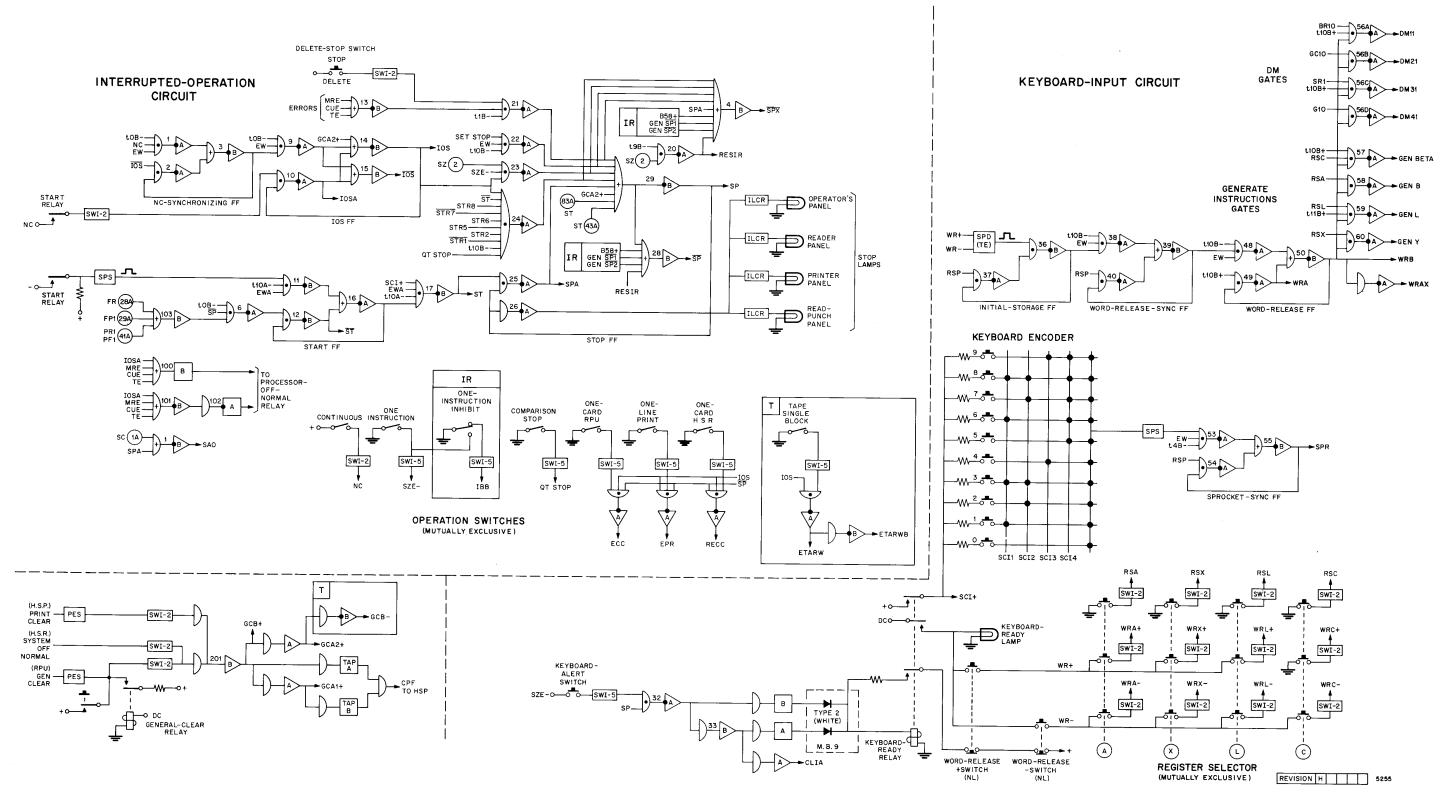


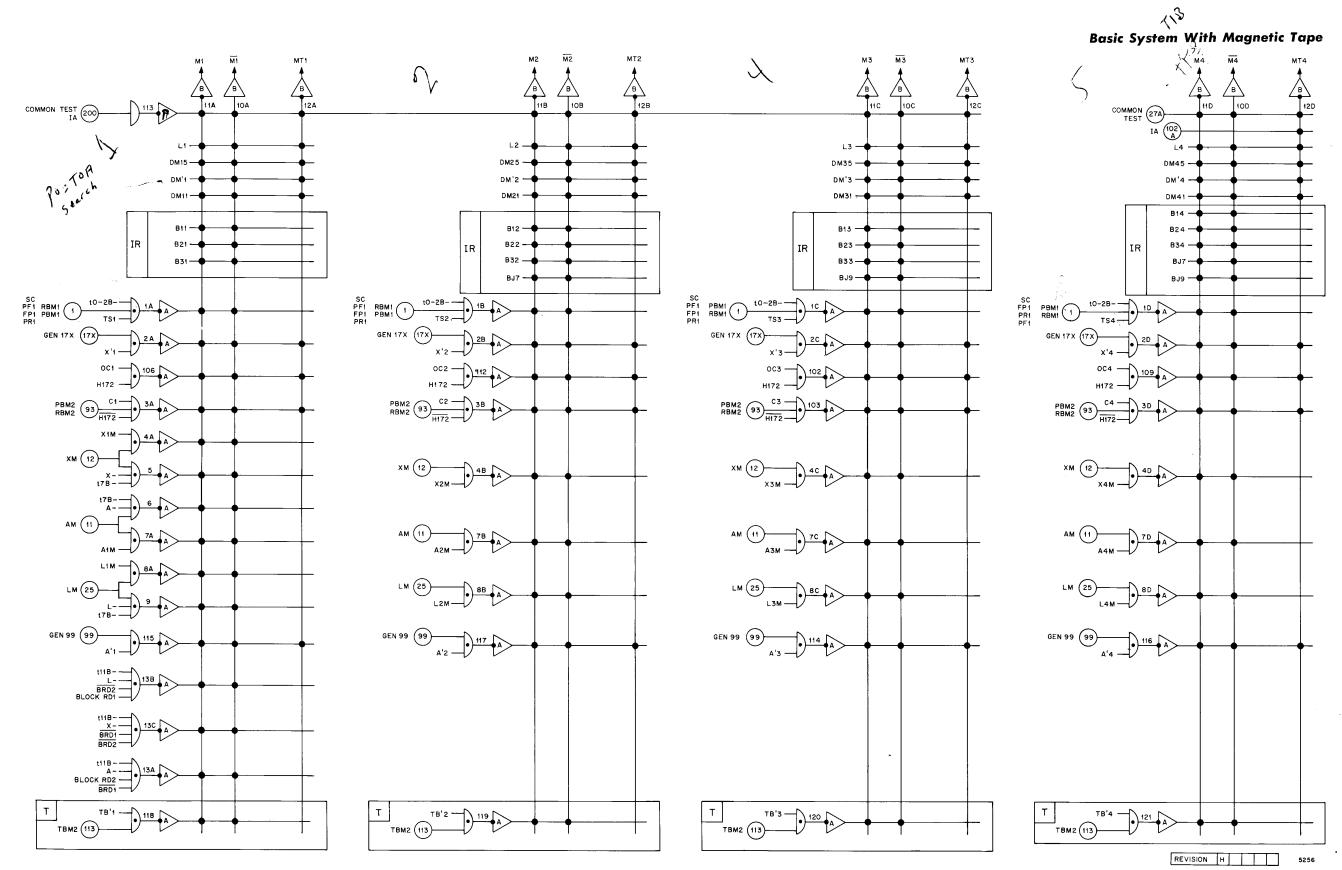




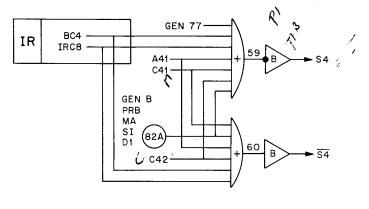


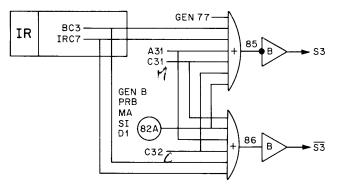


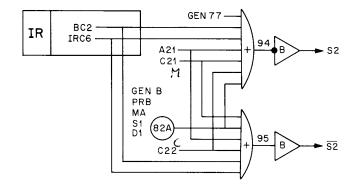


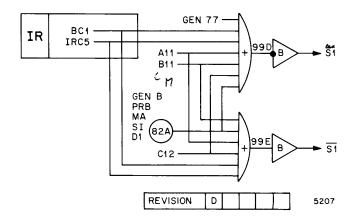


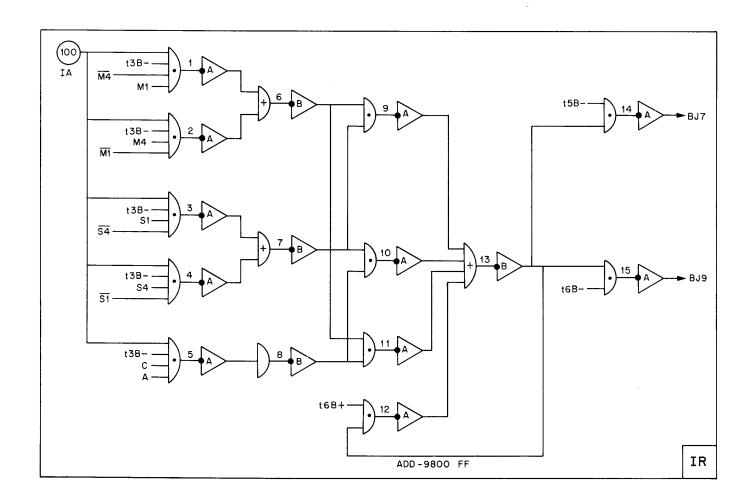
1-6A. M Buffers

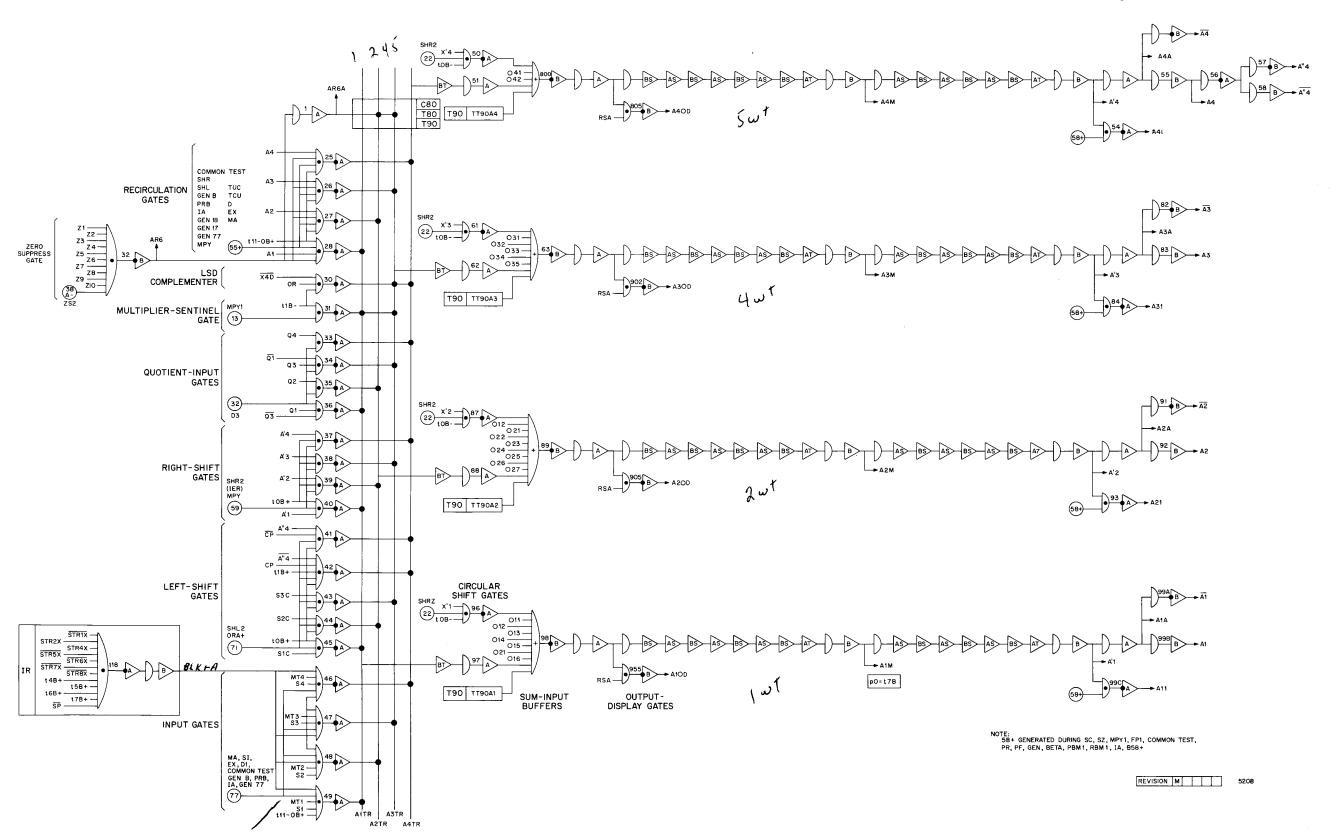




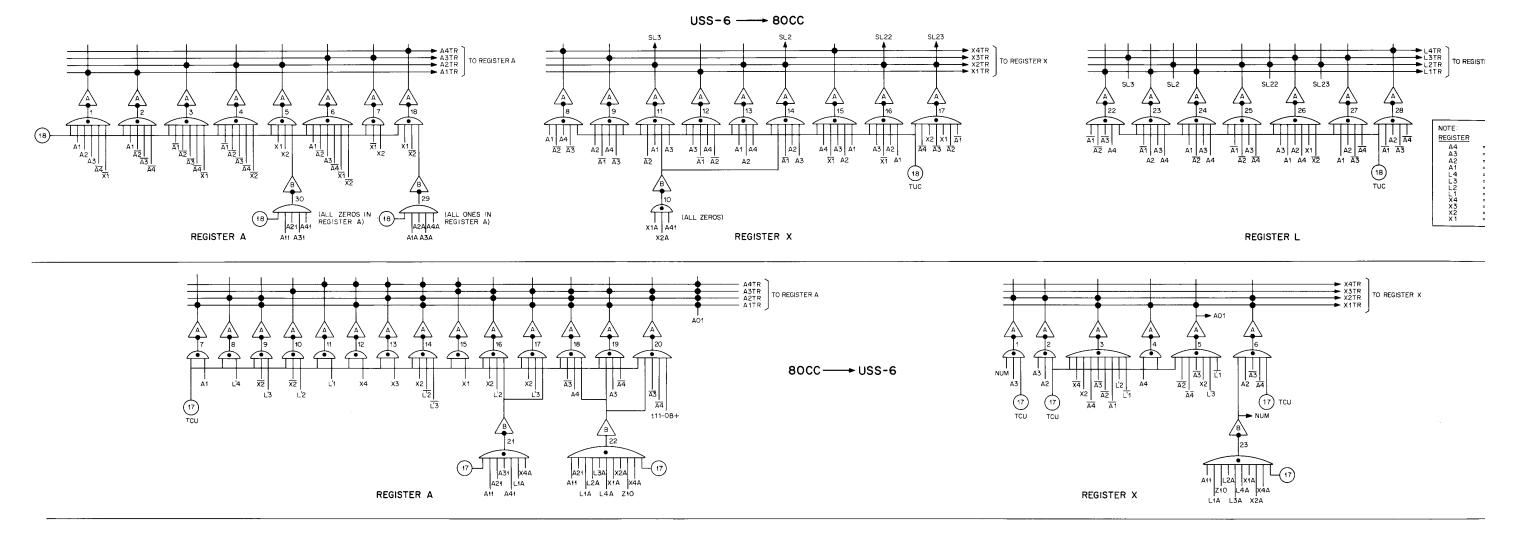


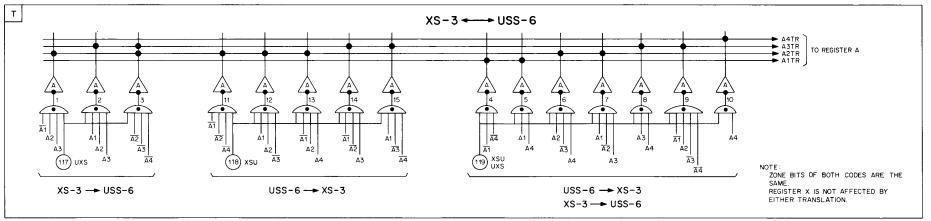




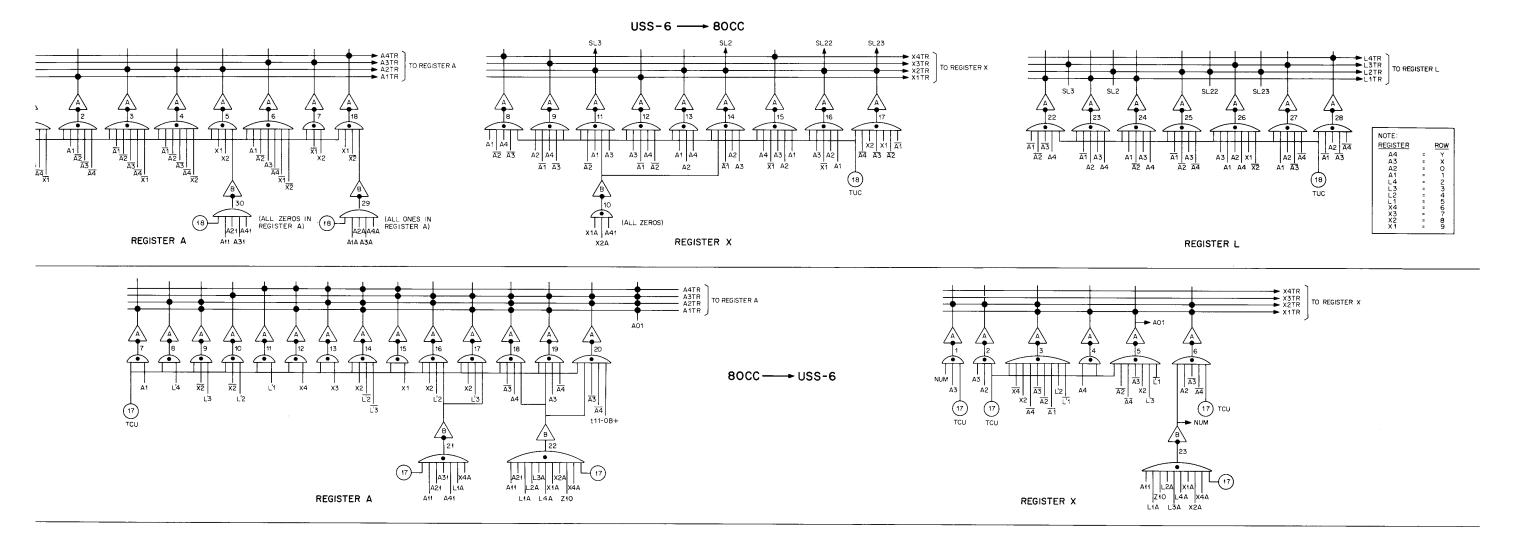


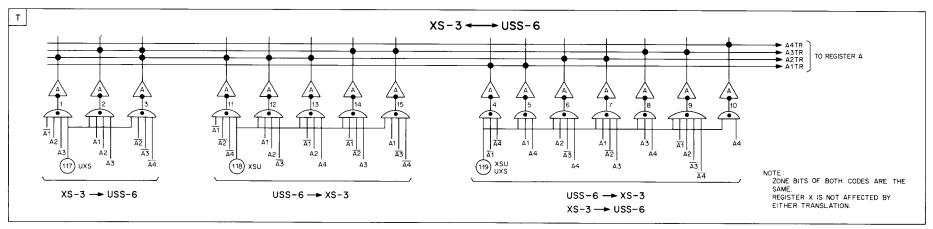
#### Basic System With Magne



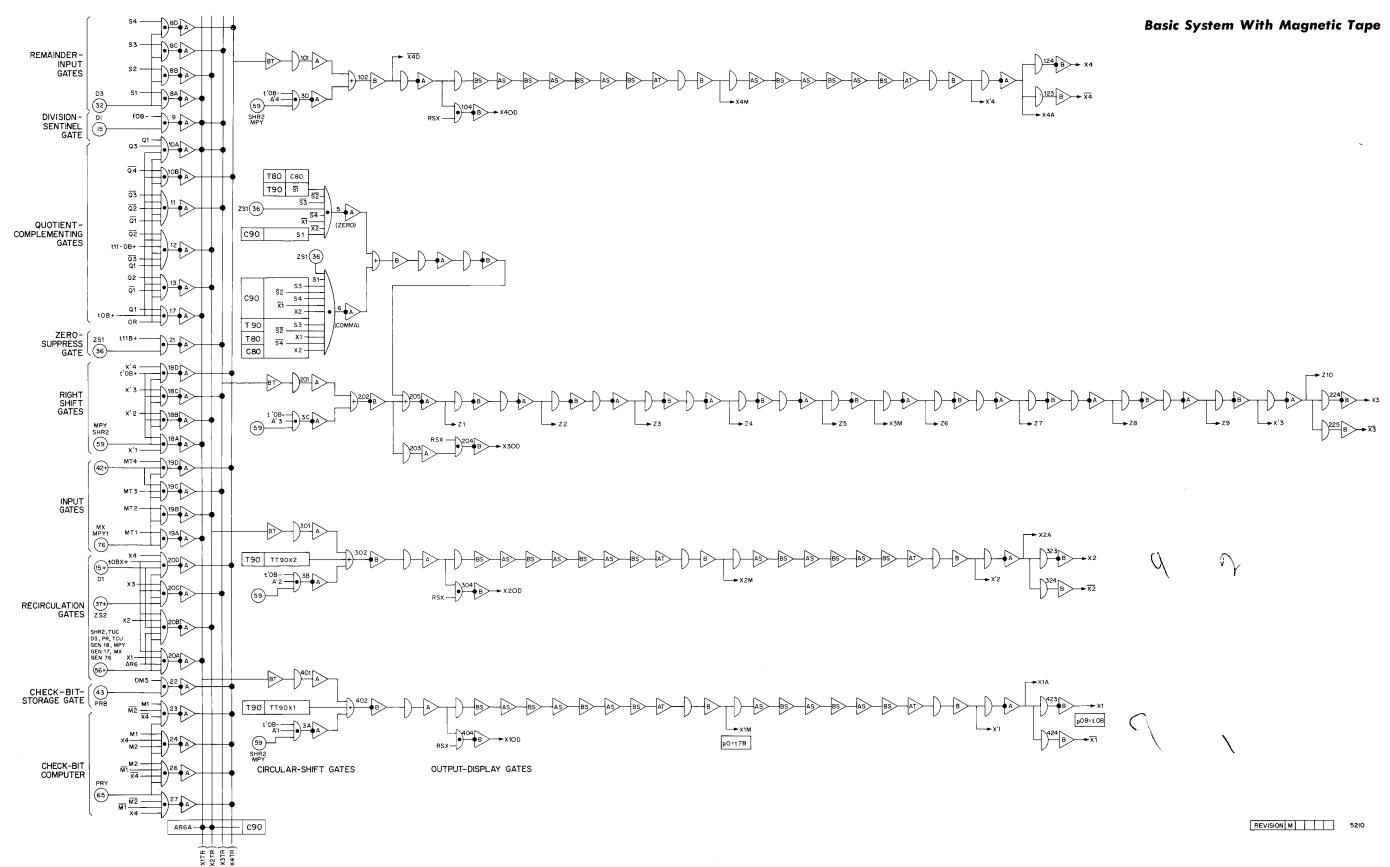


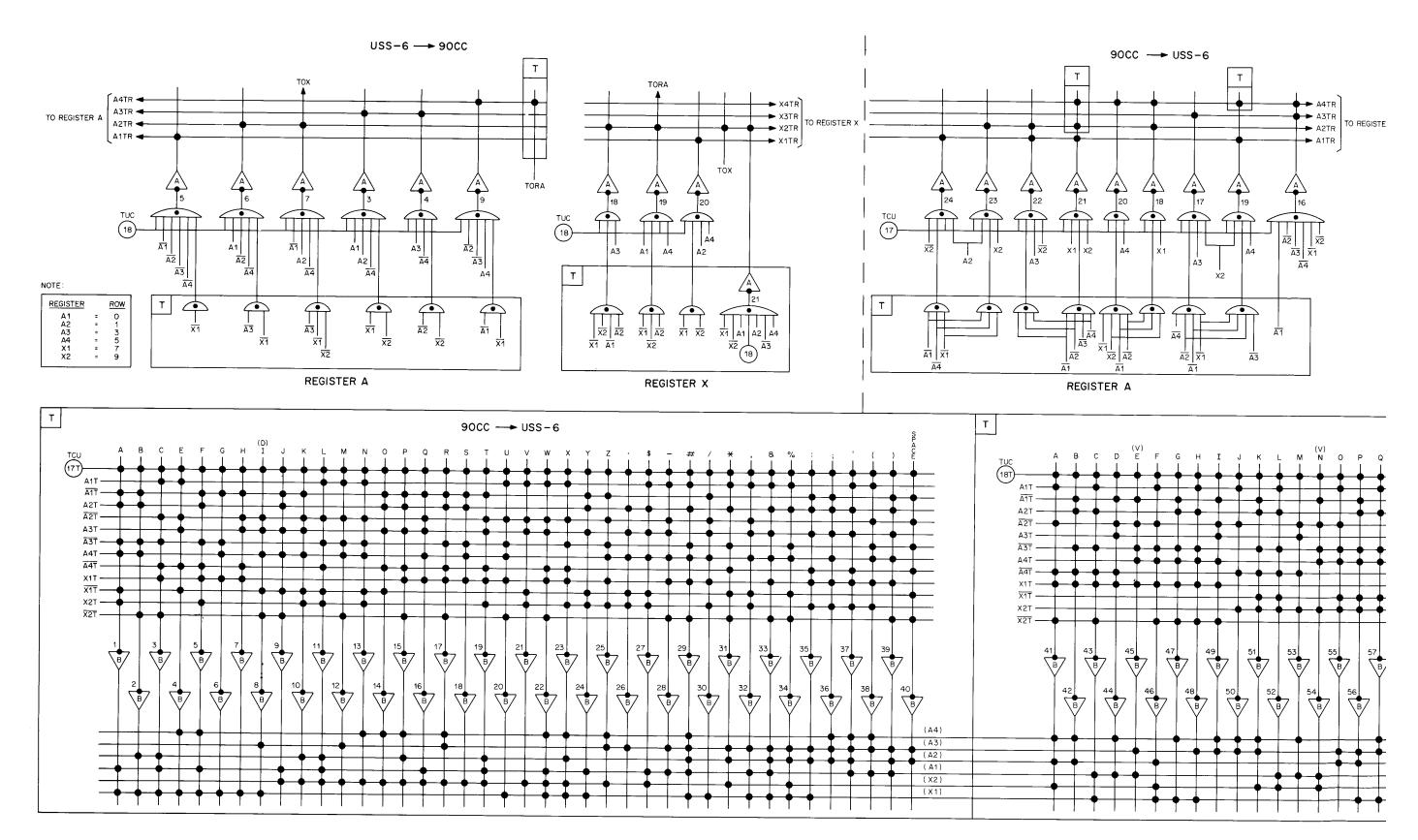
REVISION



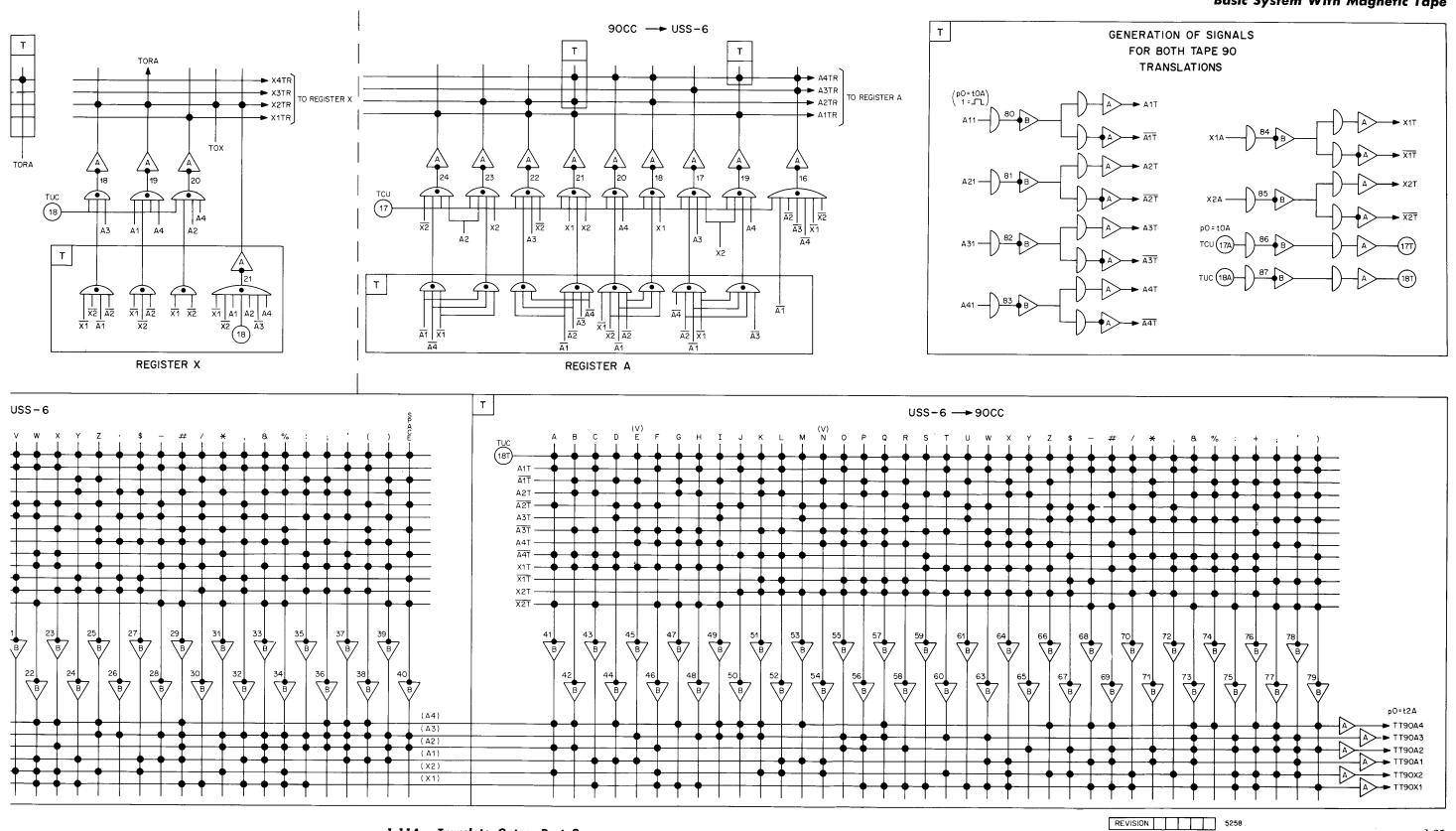


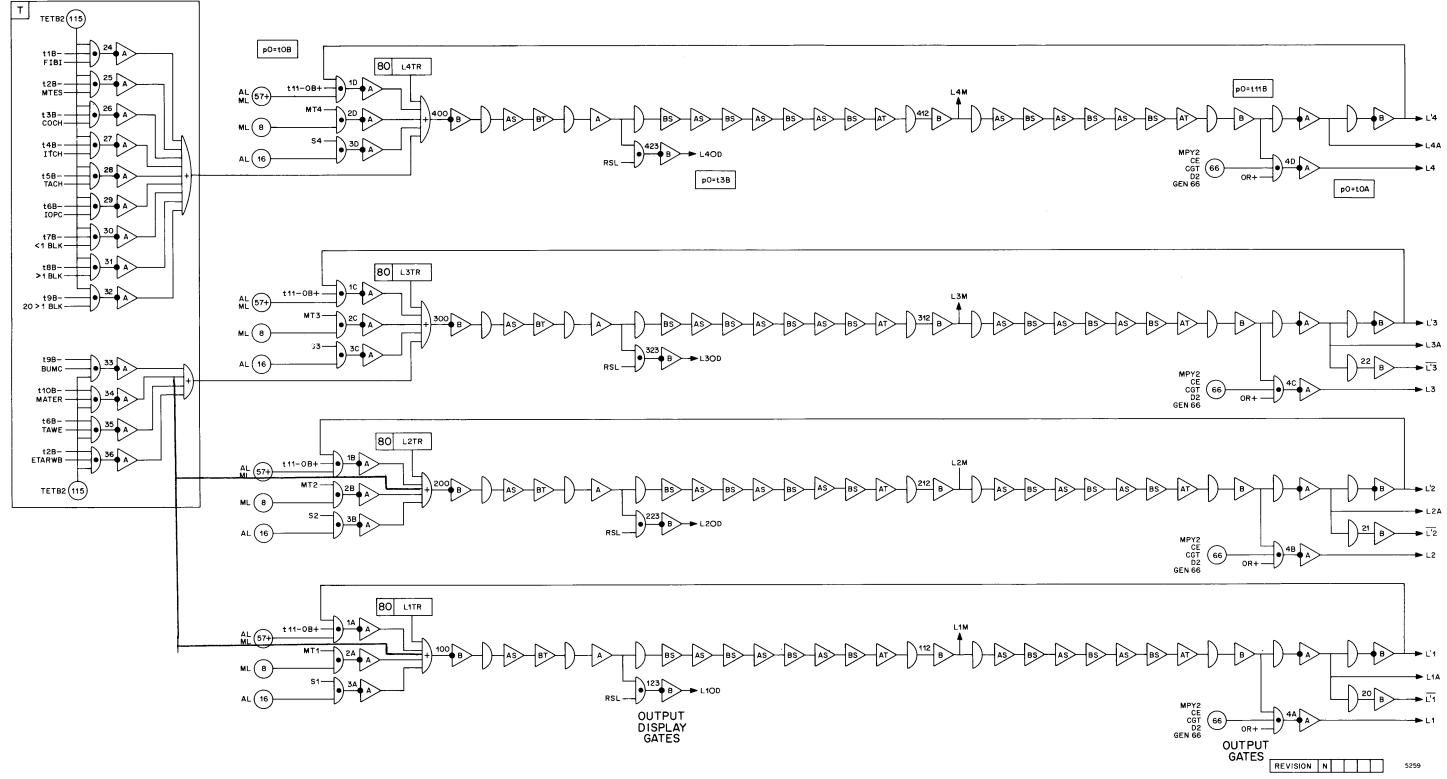
REVISION 5257

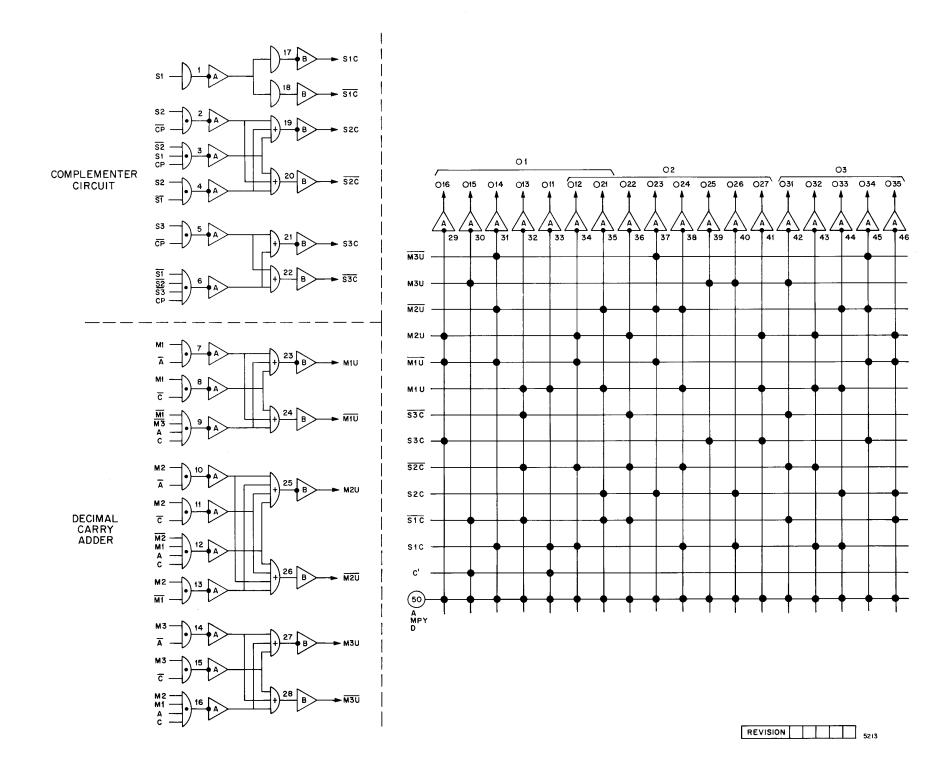




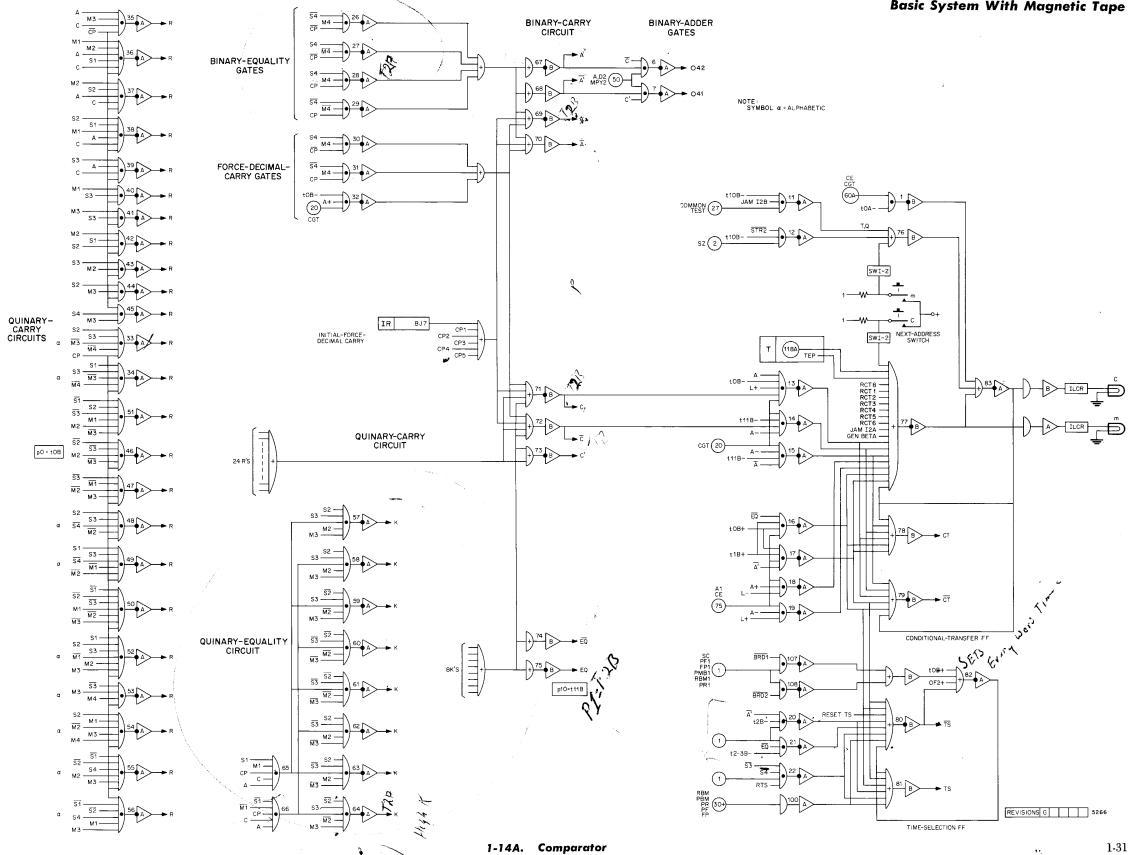
1-11A. Translate Gates, Part 2

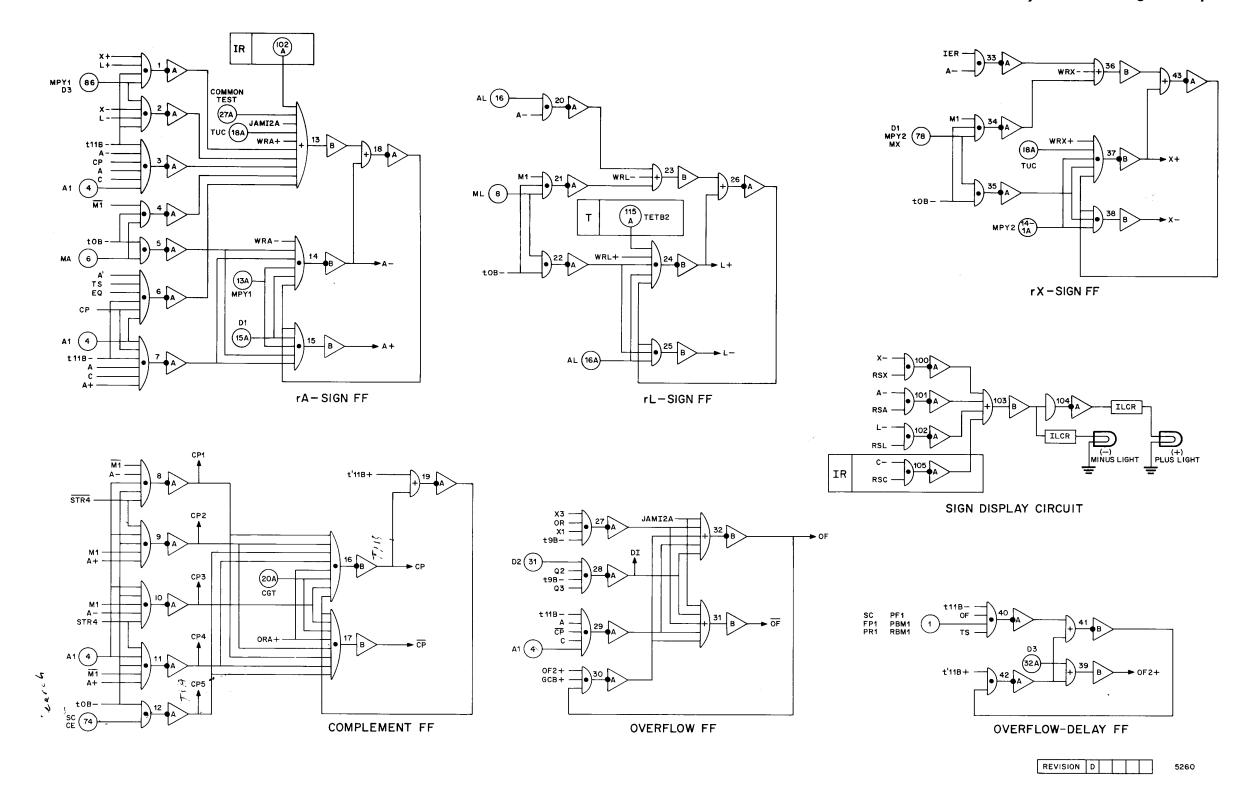




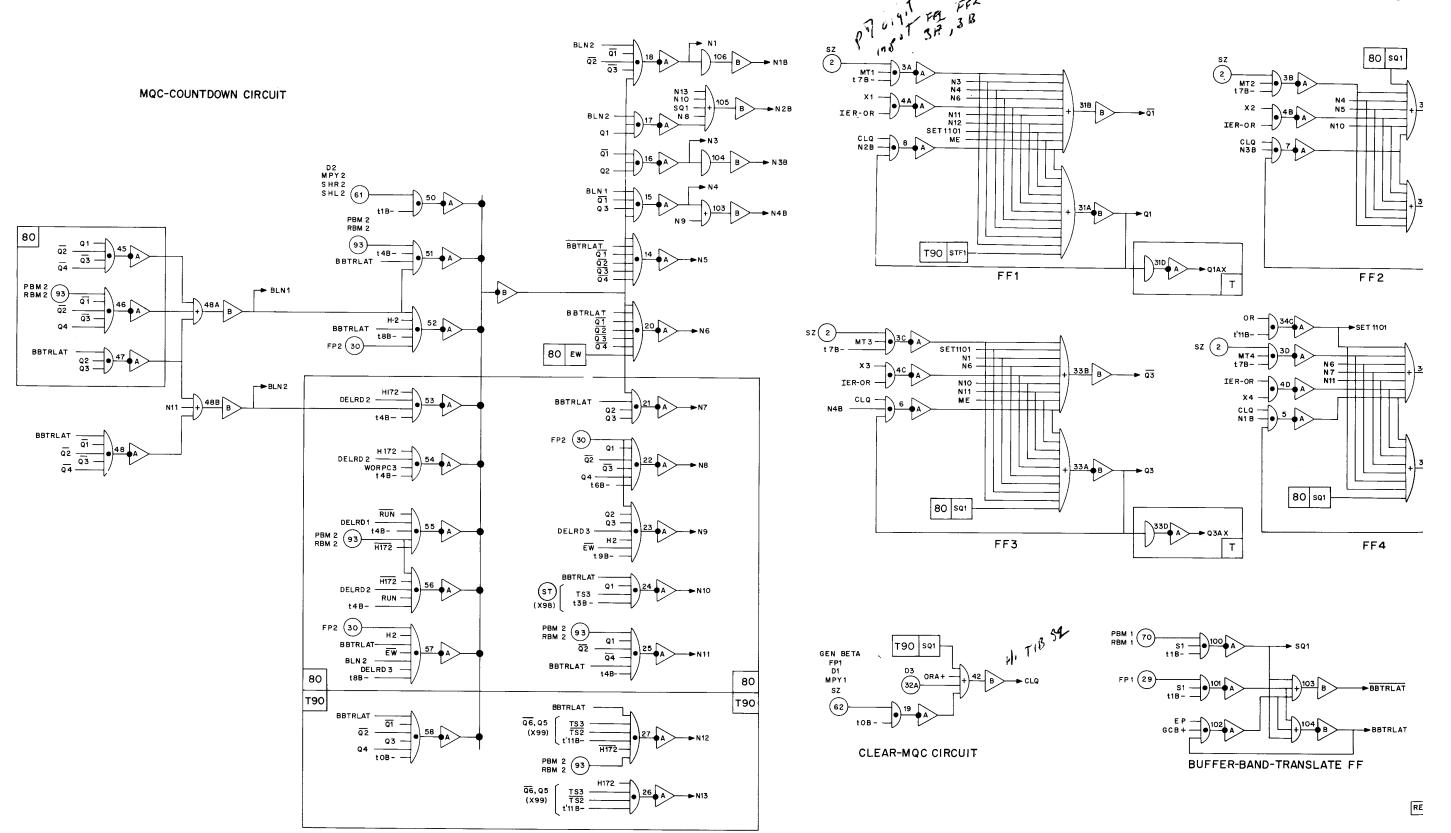


1-13A. Quinary Adder

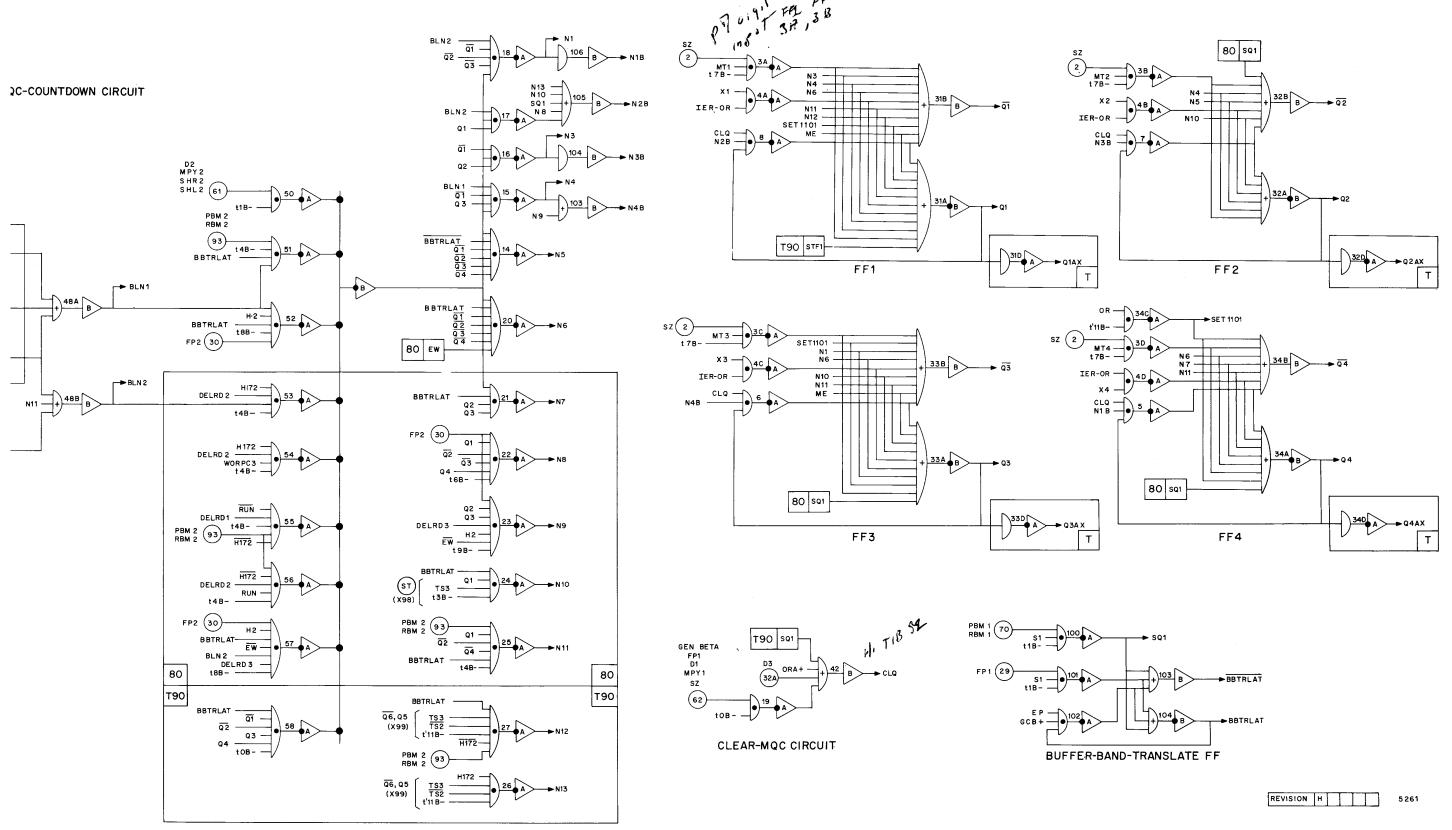


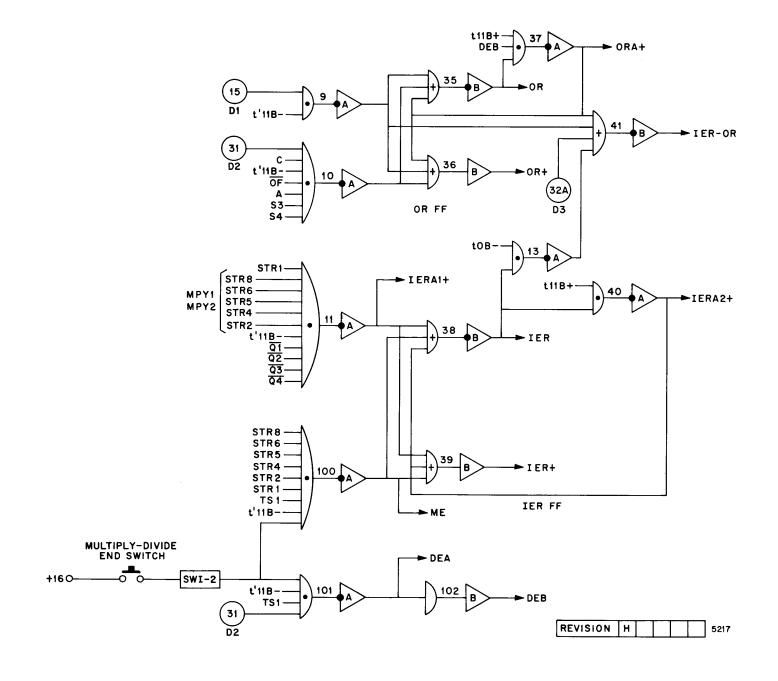


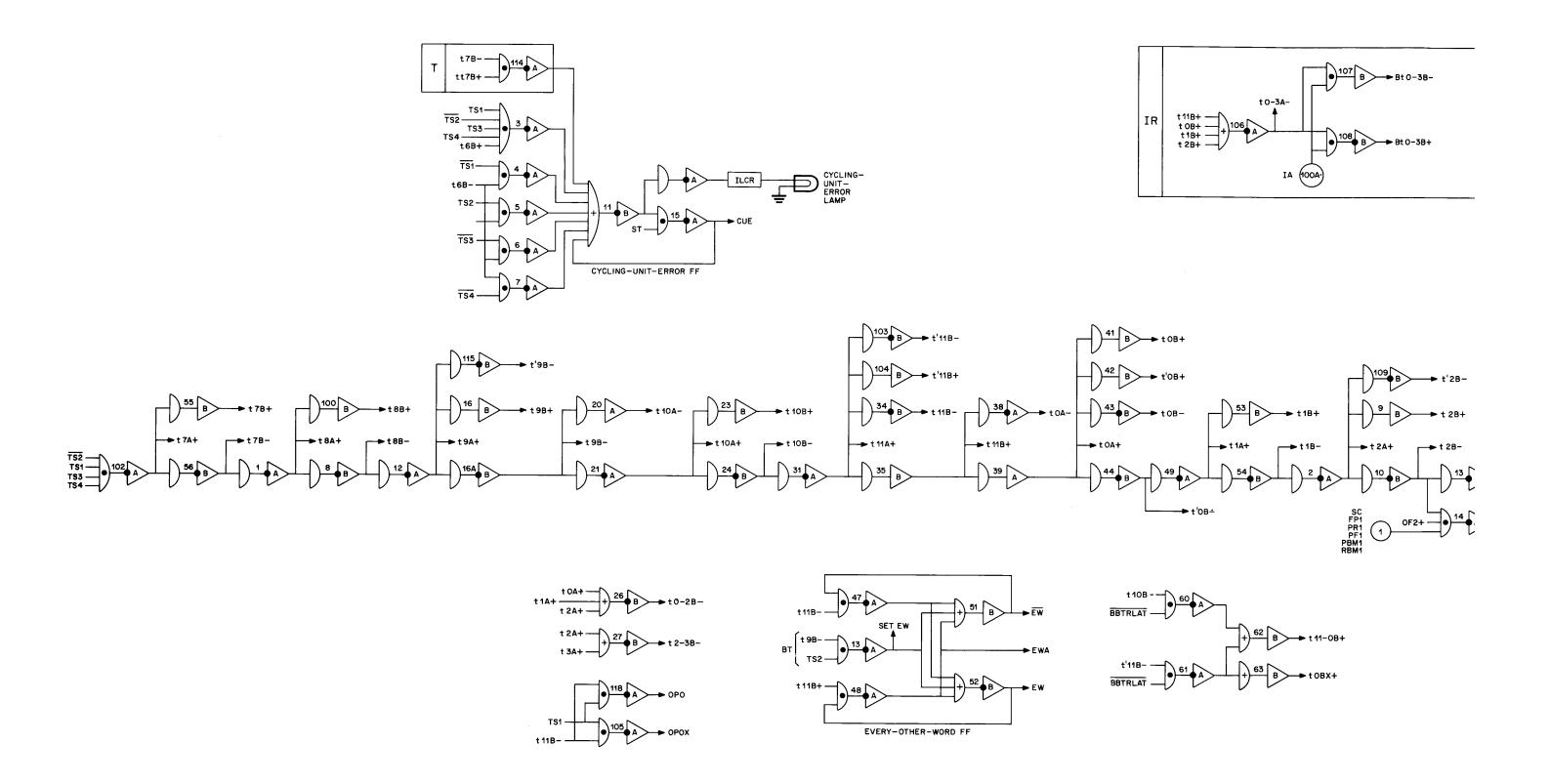




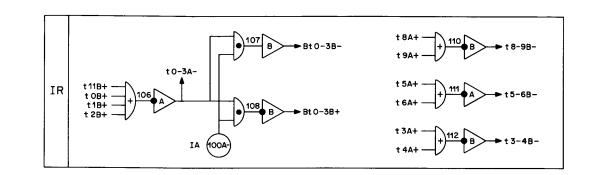
1-16A. Multiplier-Quotient Counter

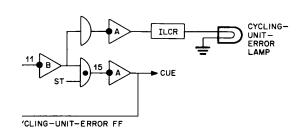


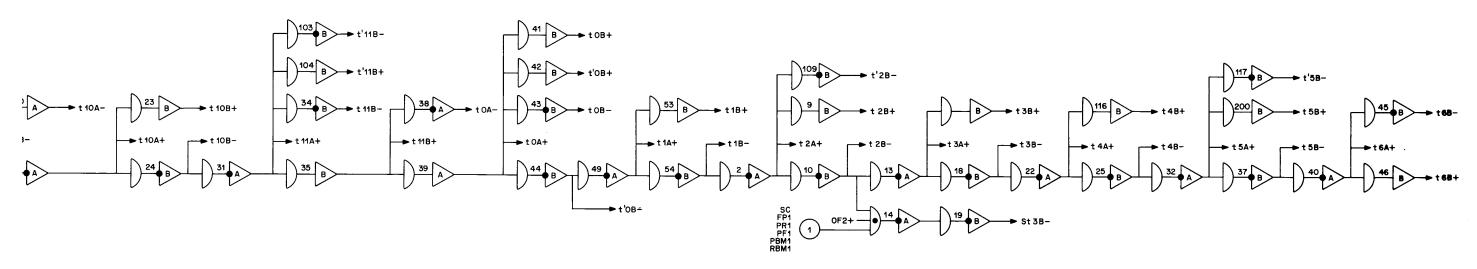


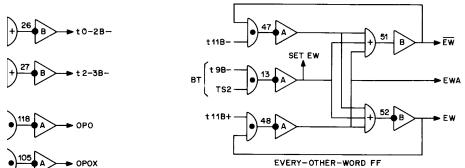


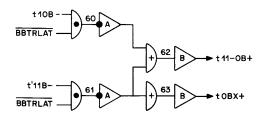
1-18A. Cycling Unit (Model 131)



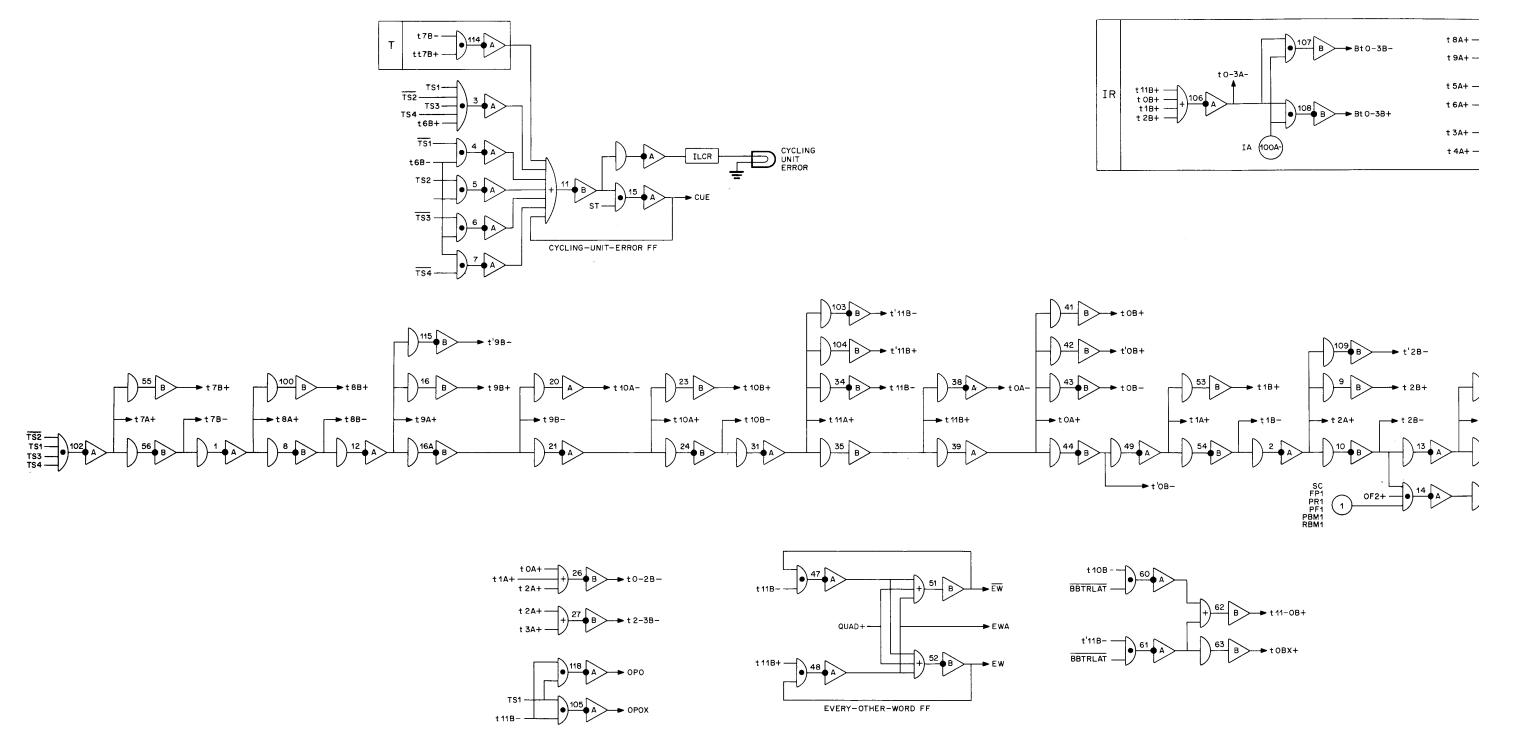




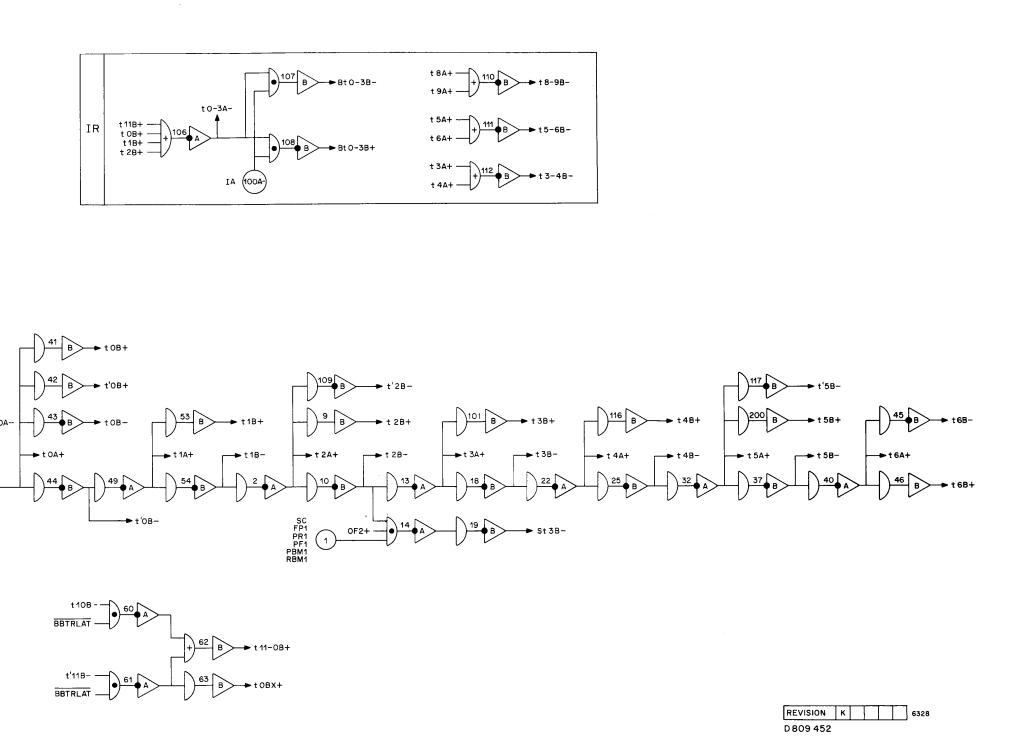


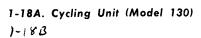


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1-18A. Cycling Unit (Model 130)

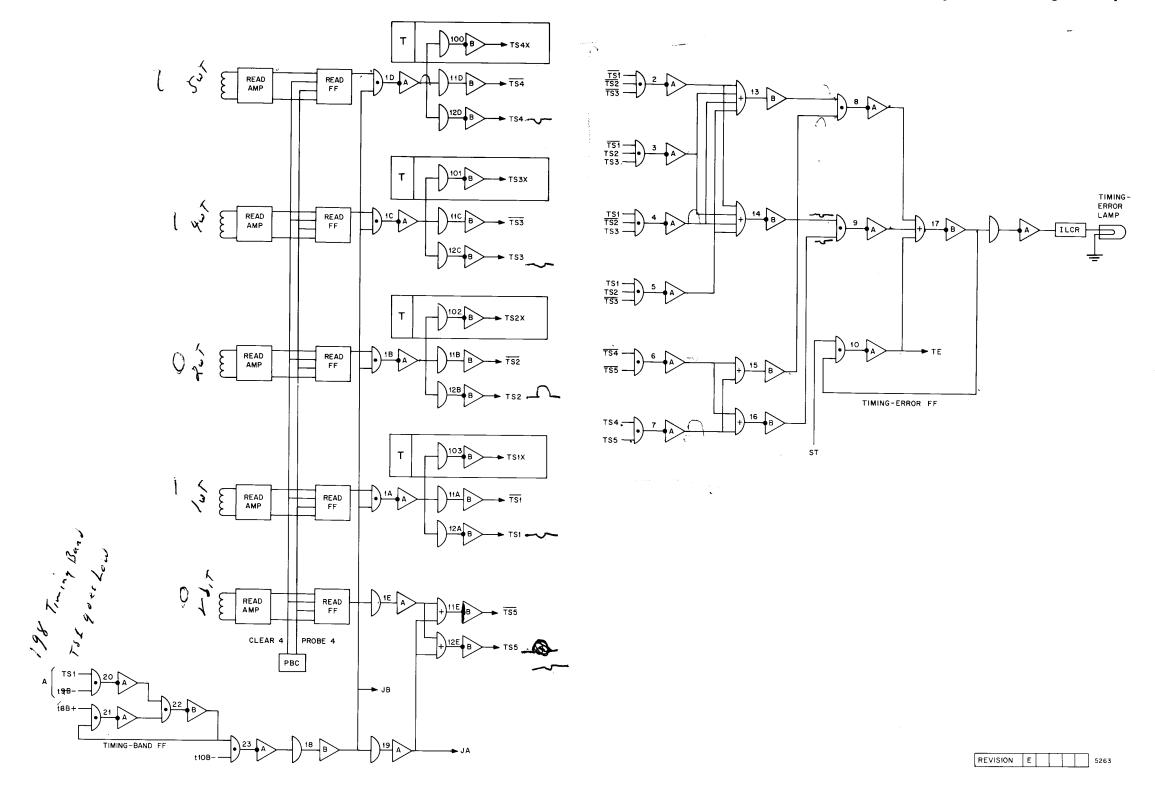


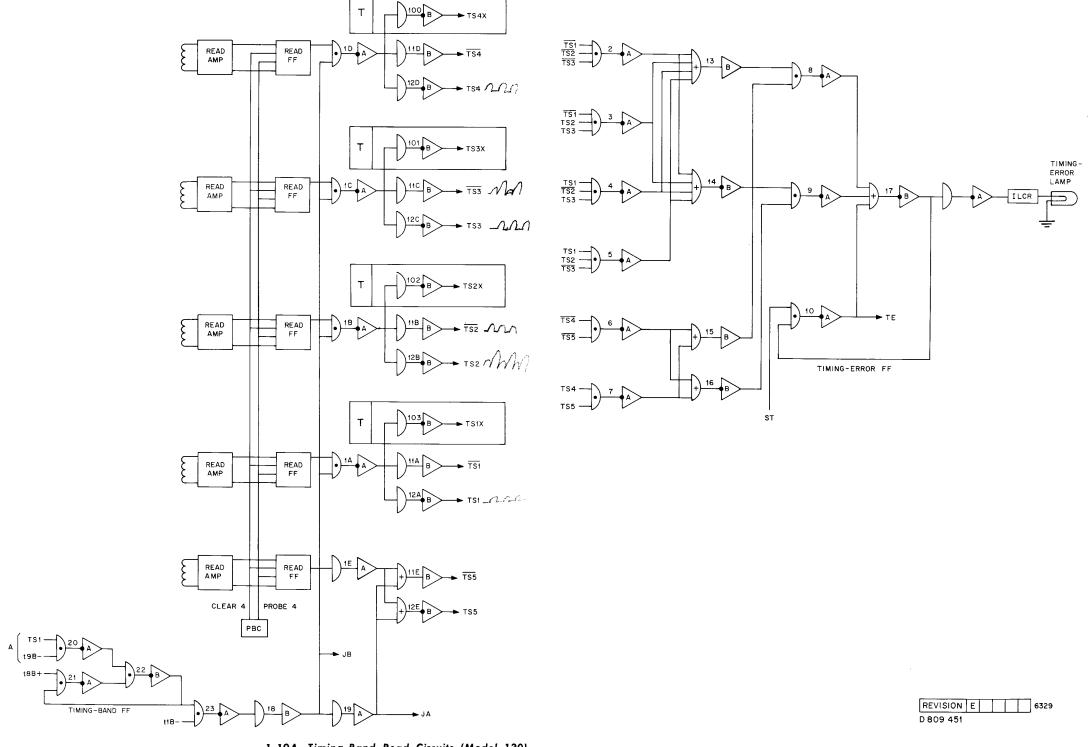


QUAD+-

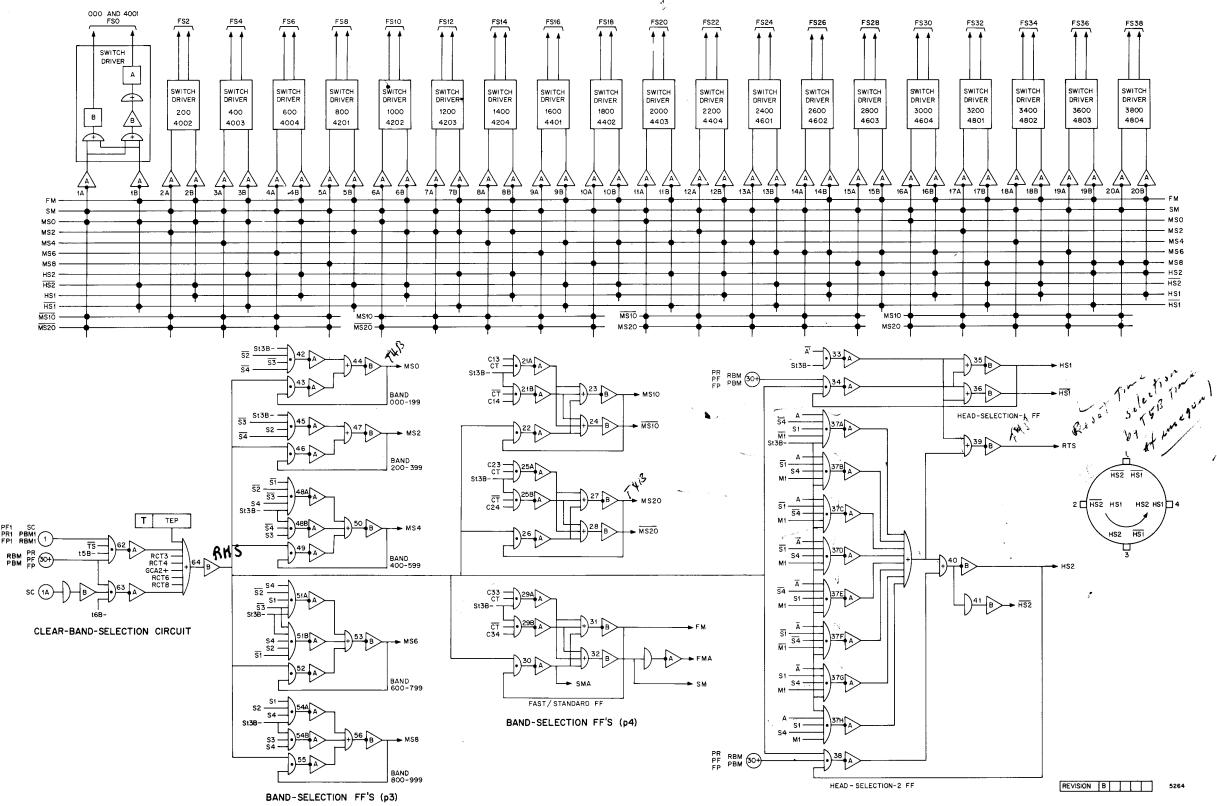
EVERY-OTHER-WORD FF

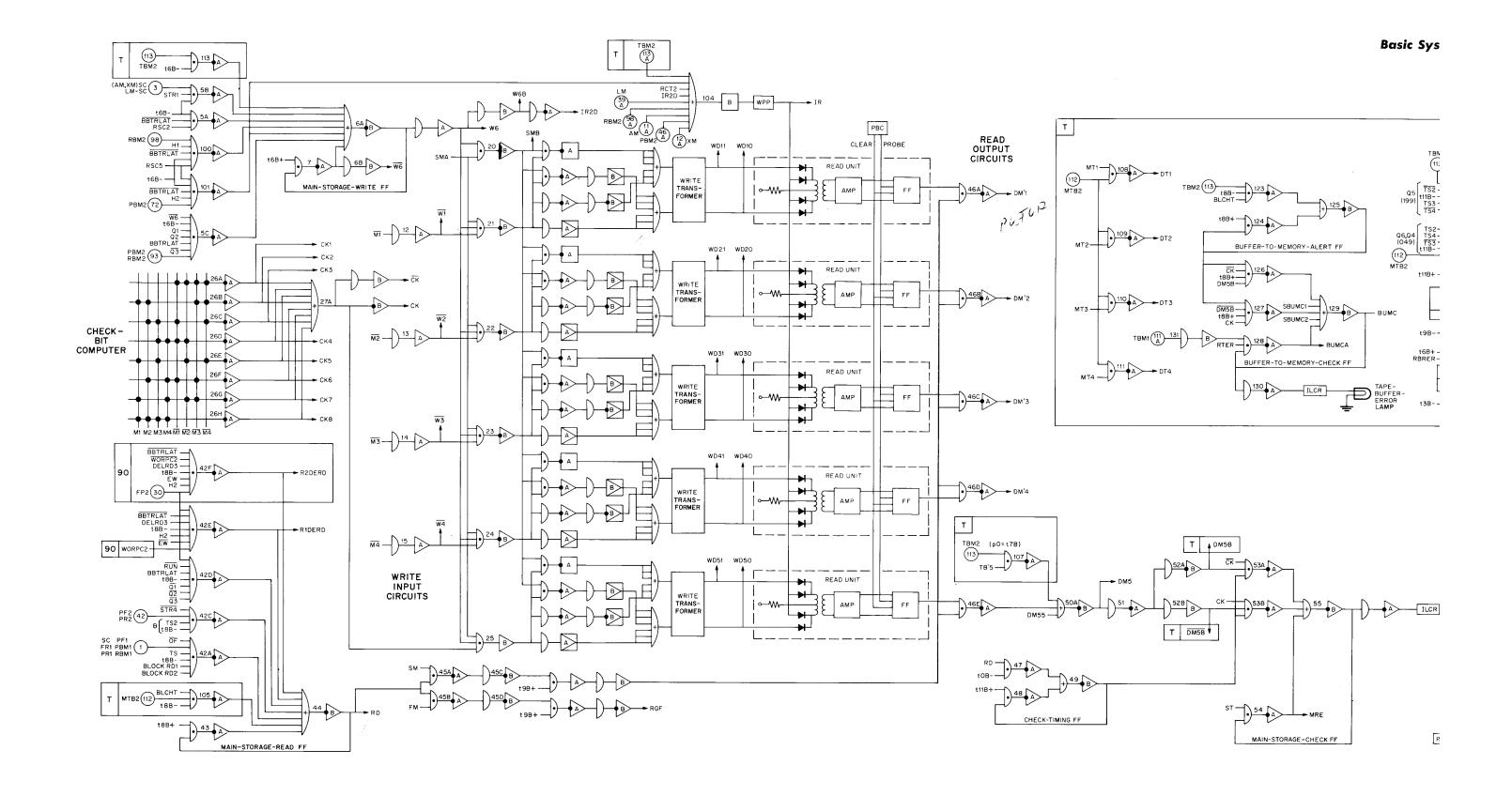
CLING-UNIT-ERROR FF

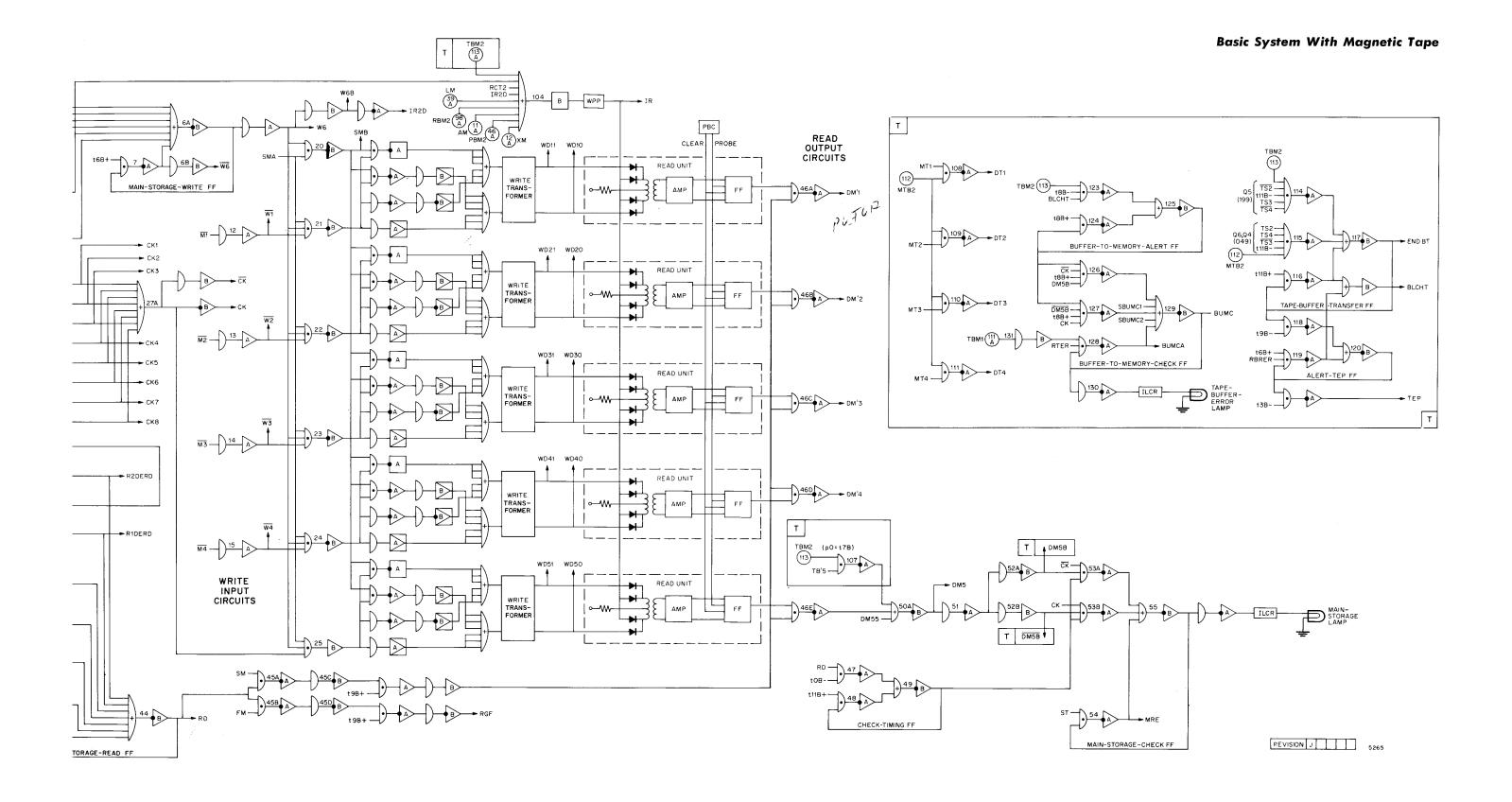


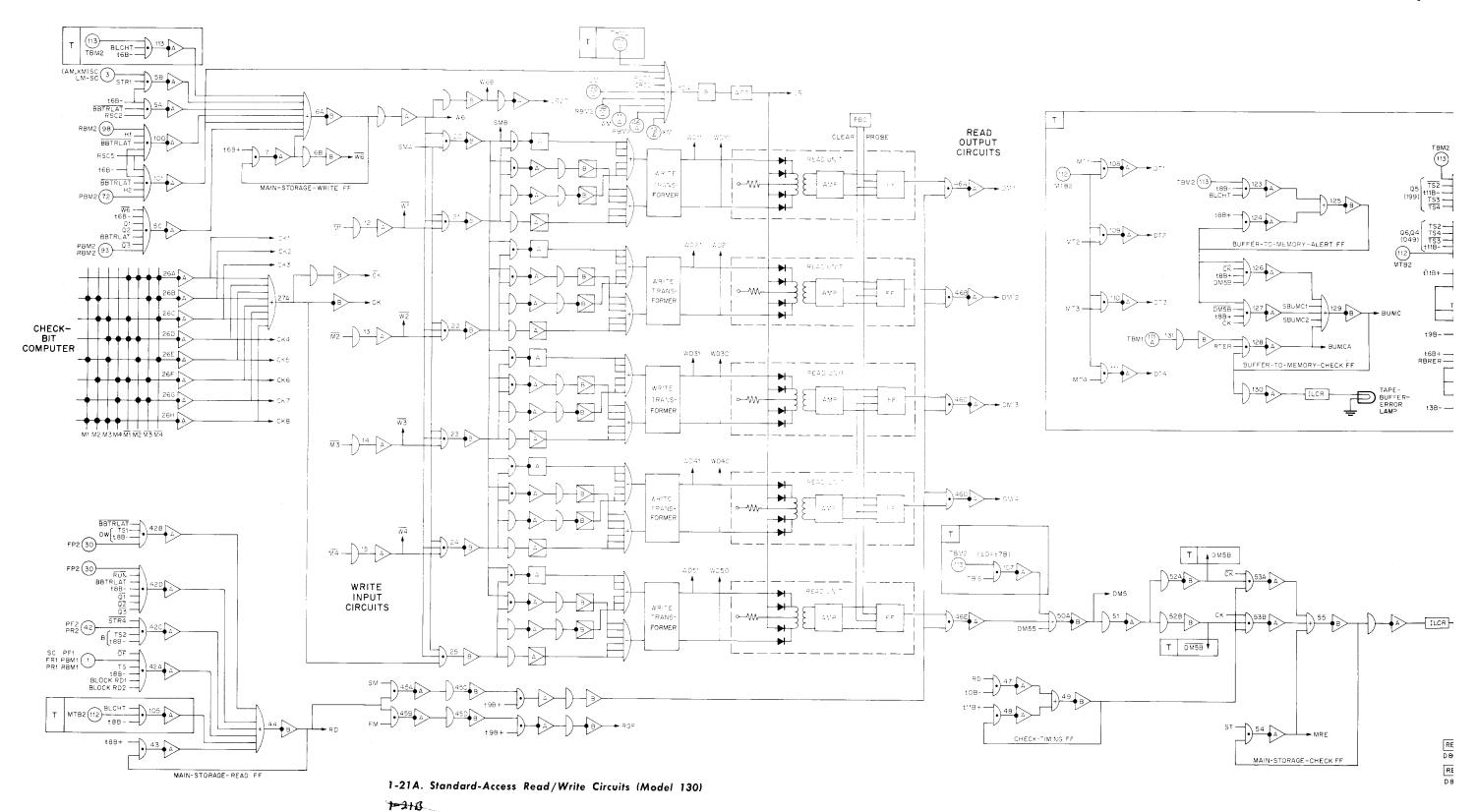


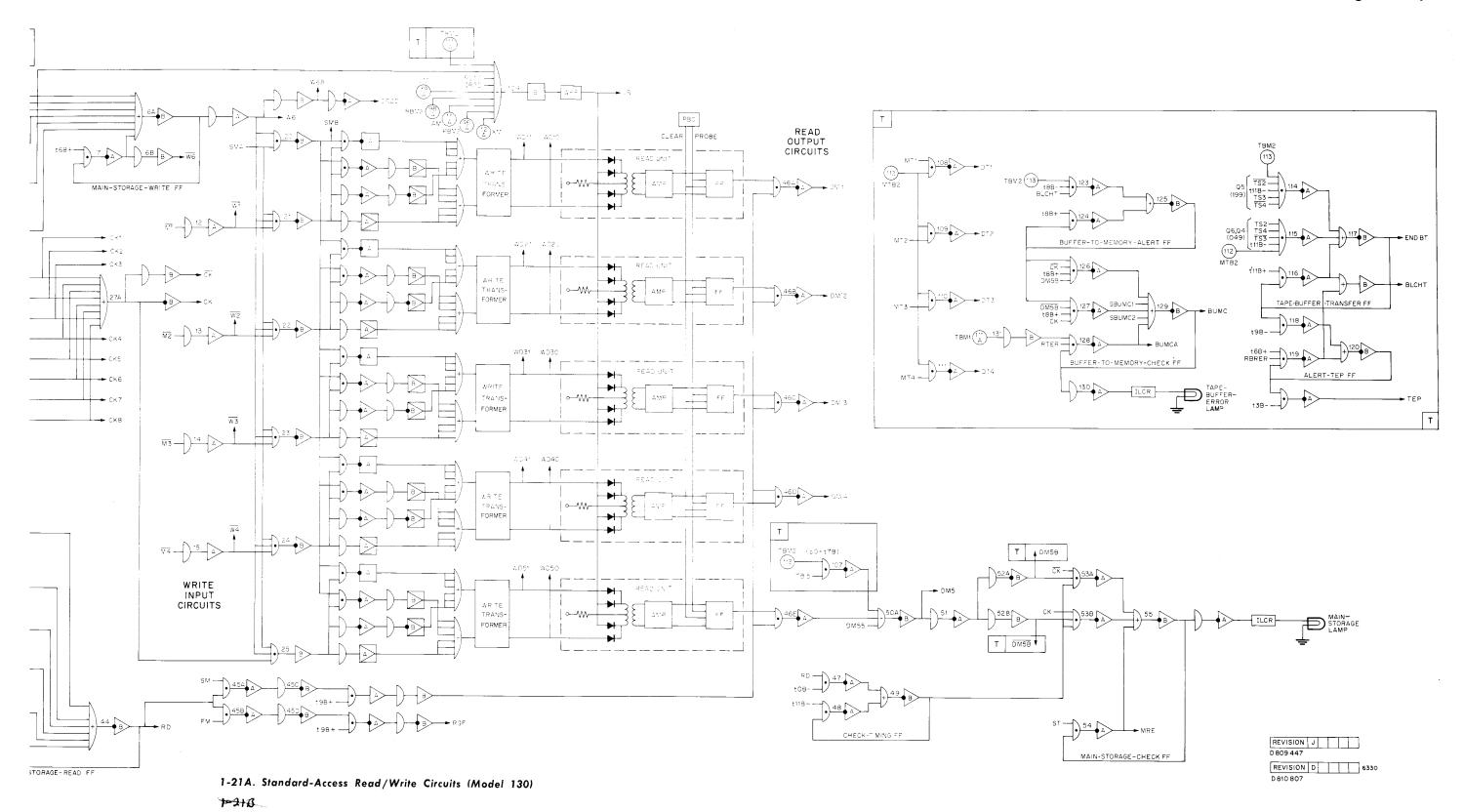
1-19A. Timing-Band Read Circuits (Model 130)

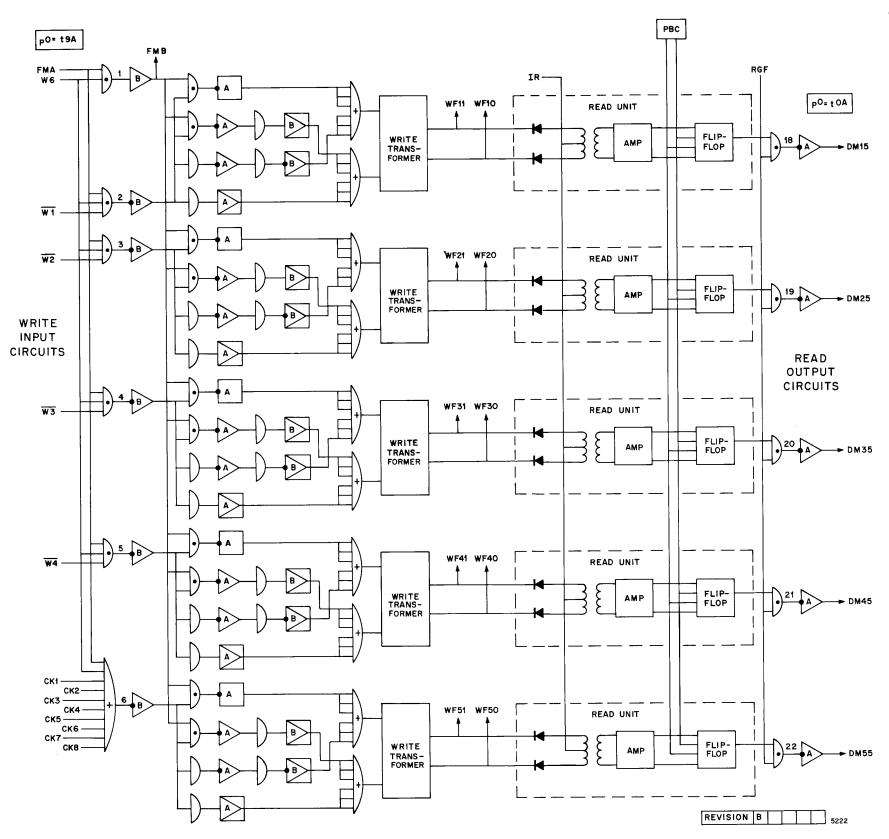




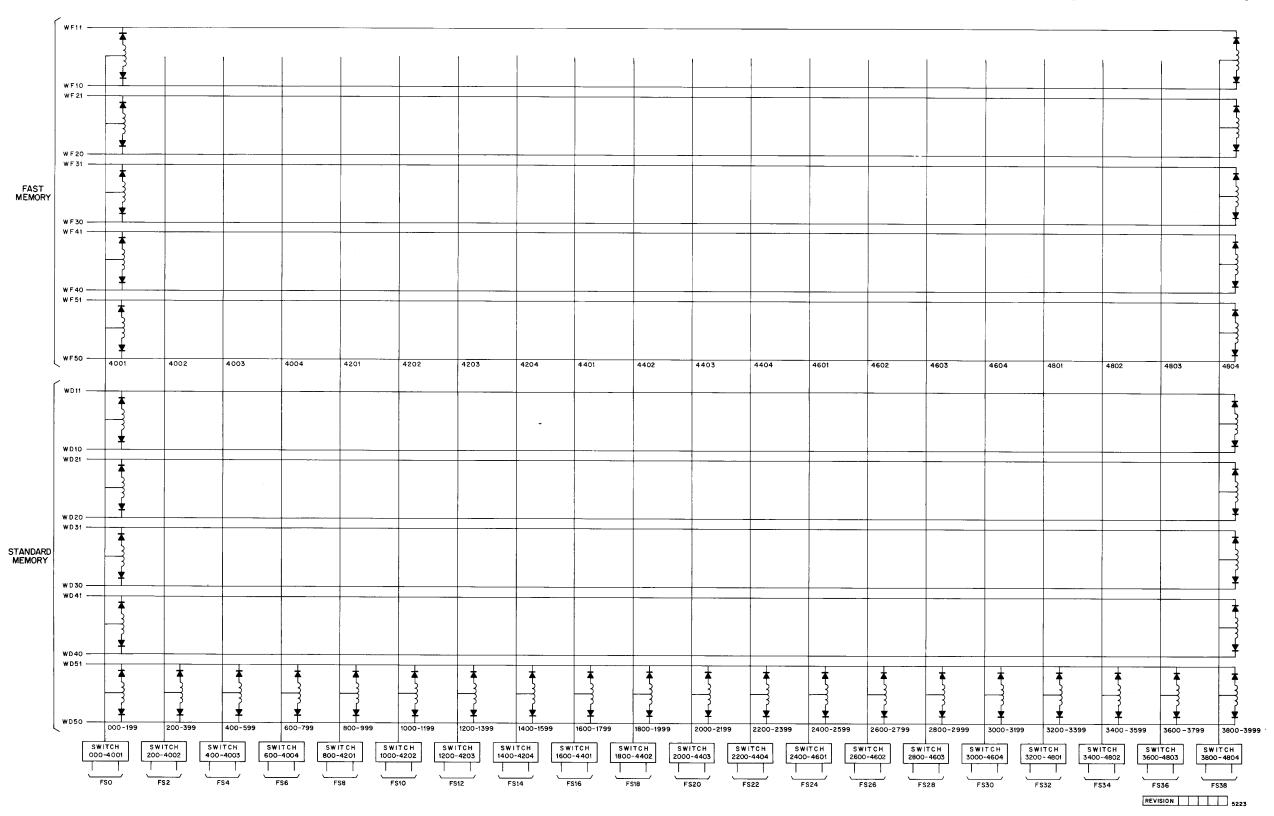


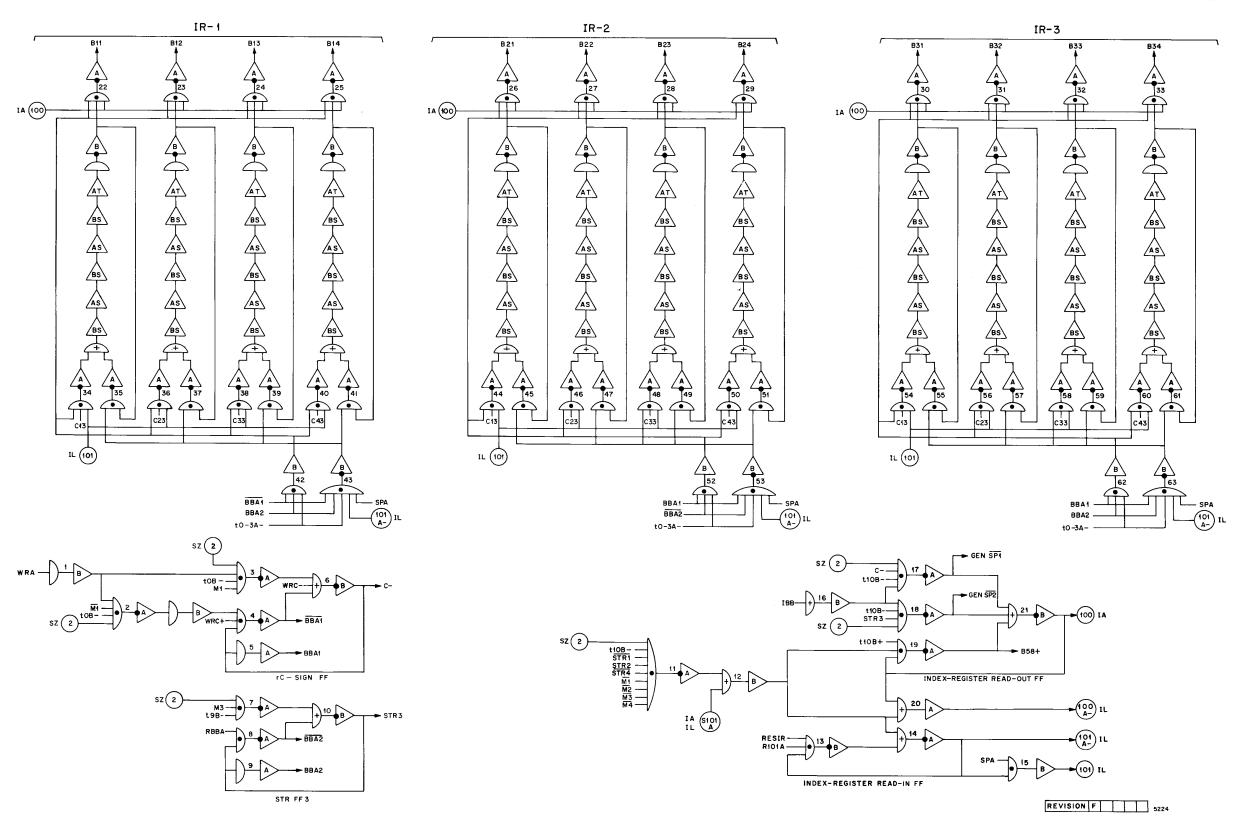


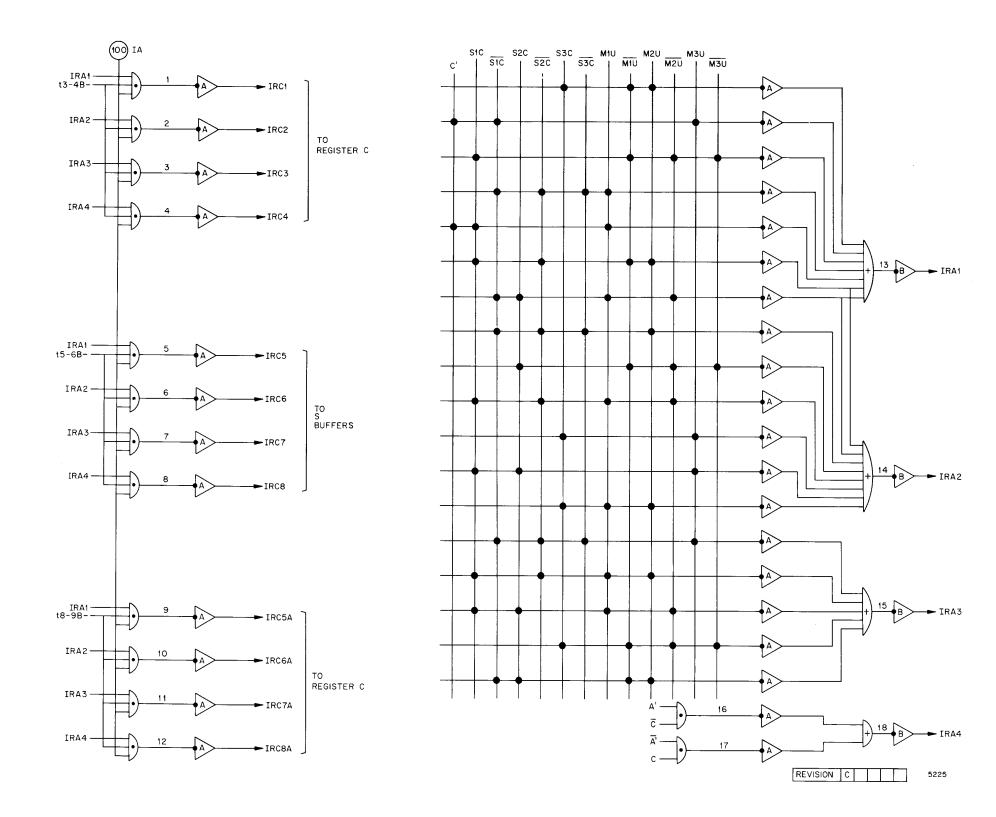


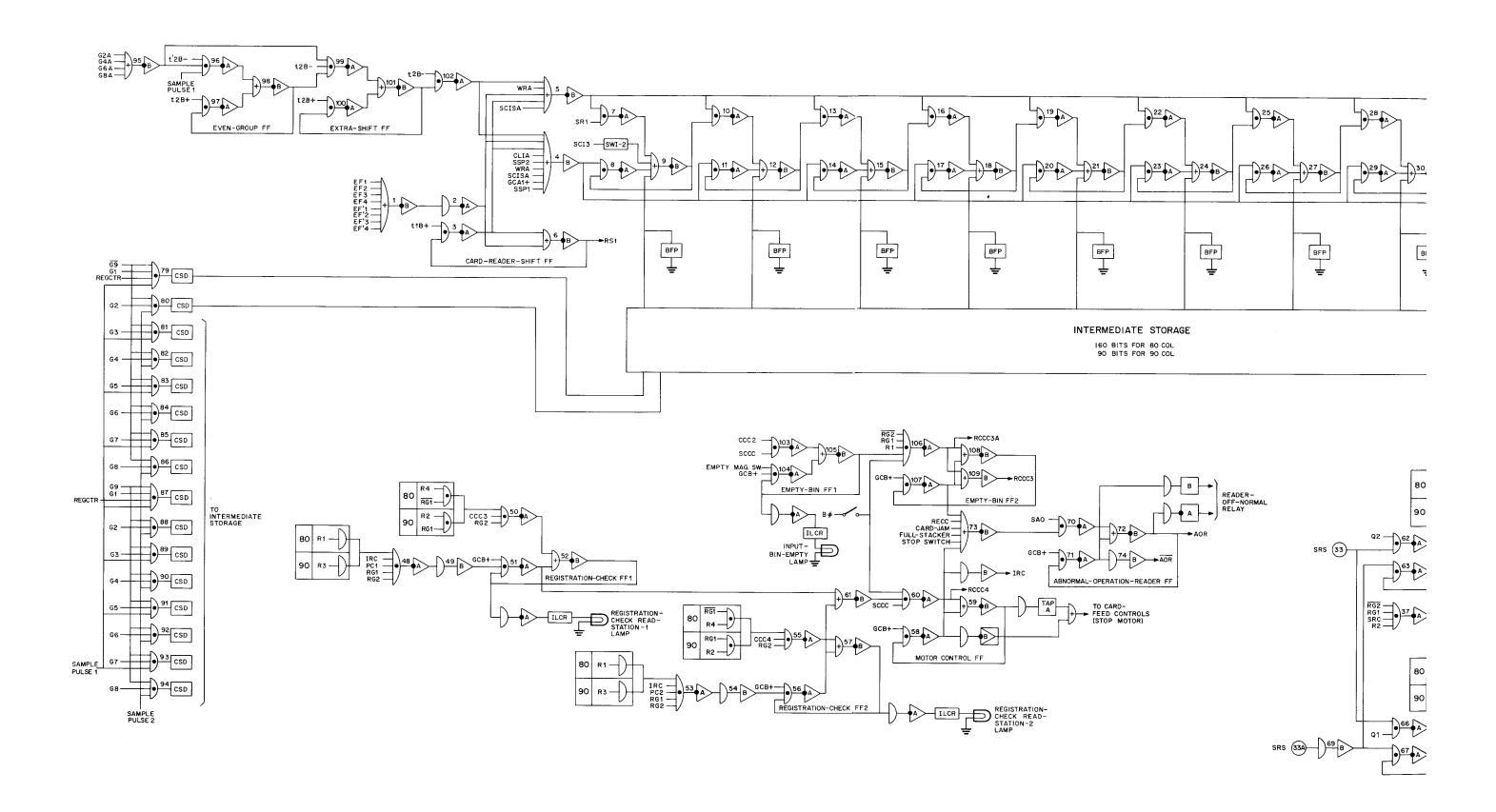


1-22A. Fast-Access Read/Write Circuits

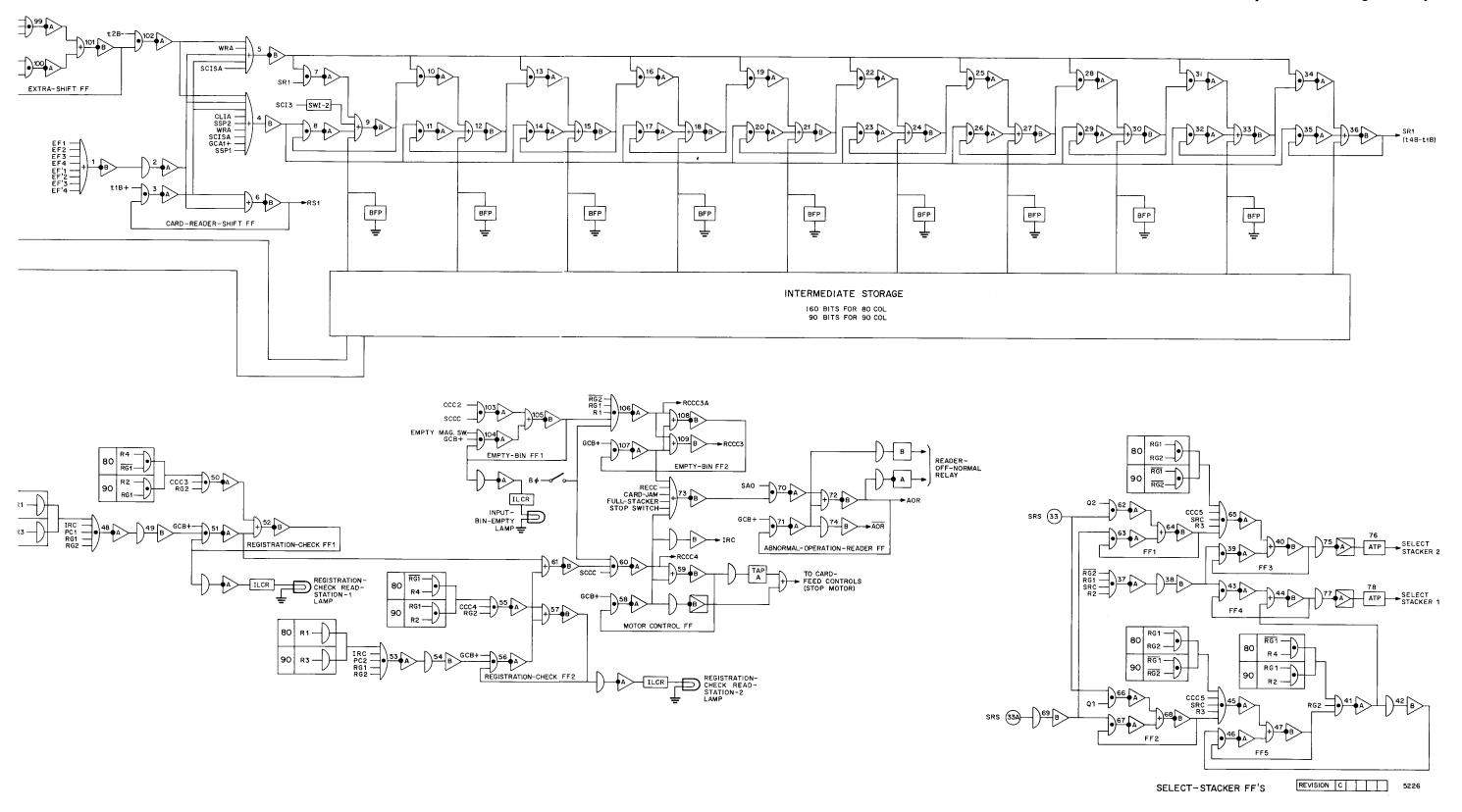


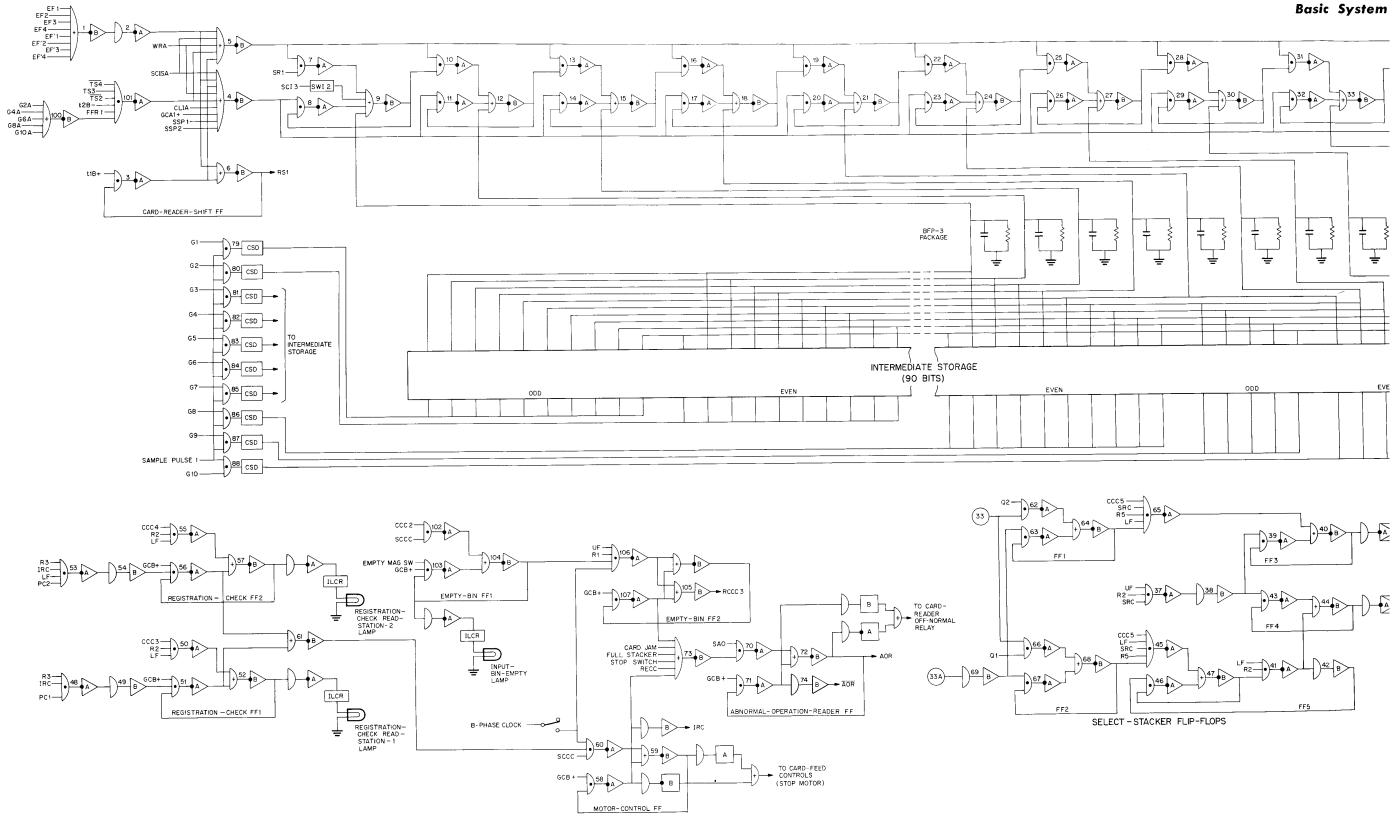




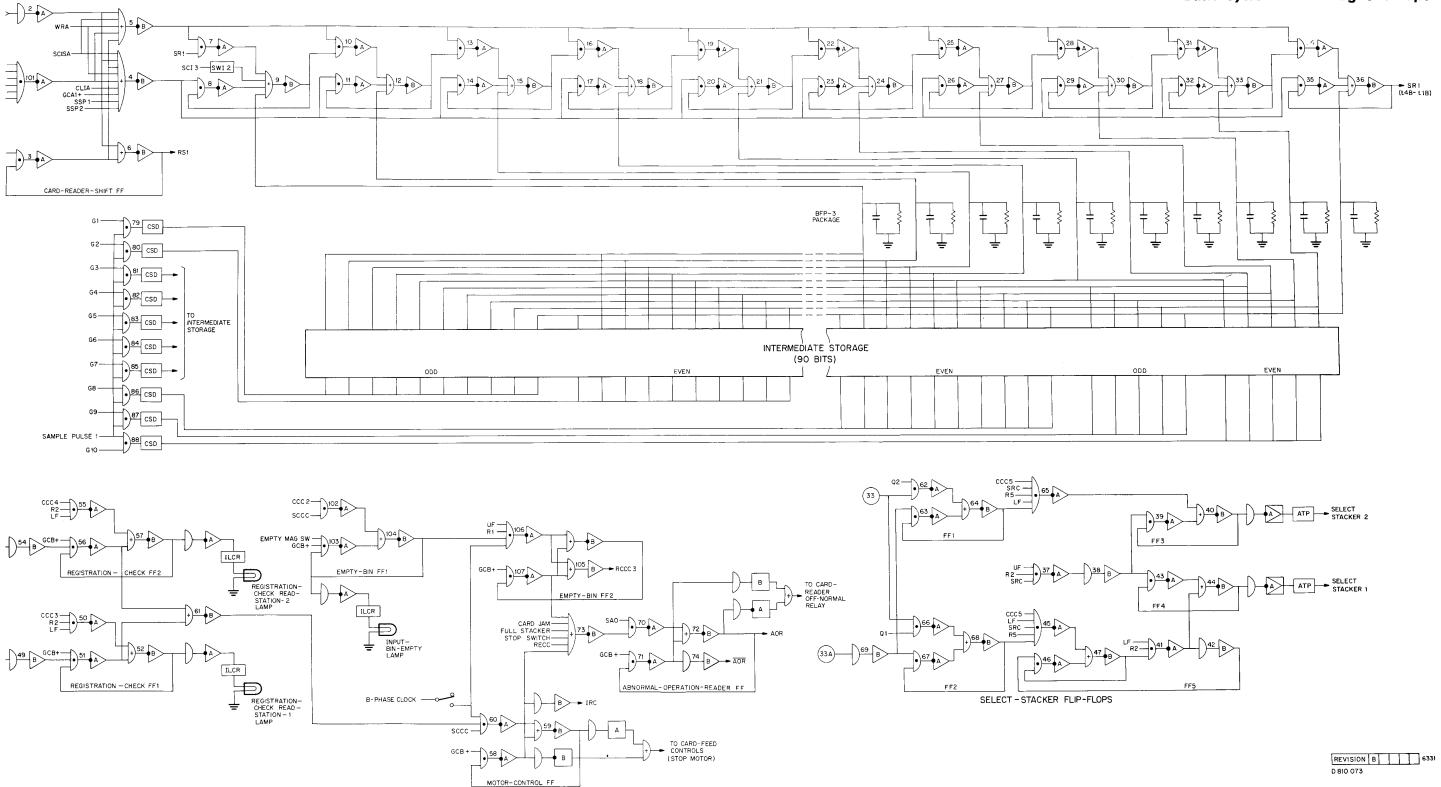


1-26A. Card-Reader Shift Register (Model 131)

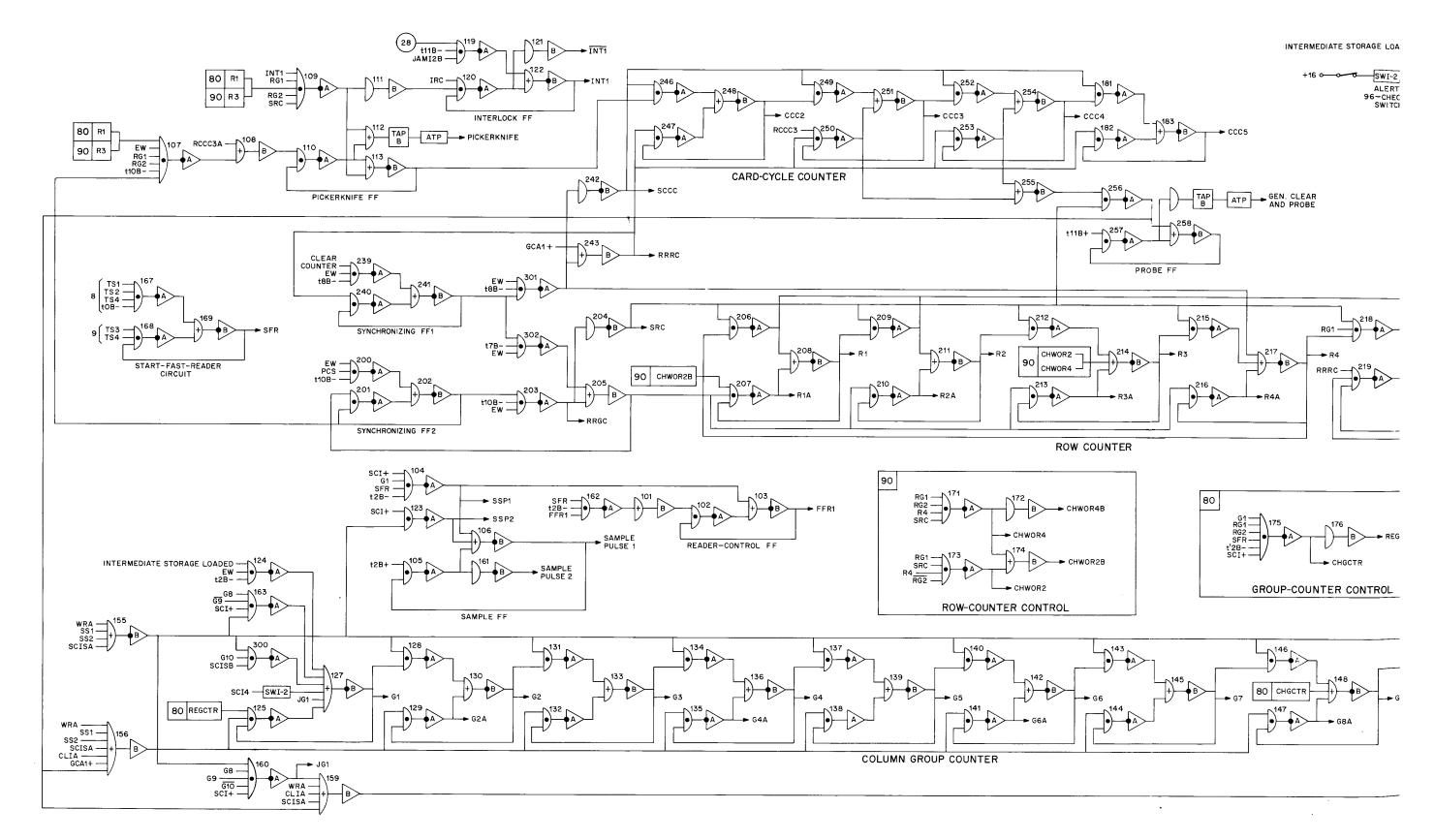




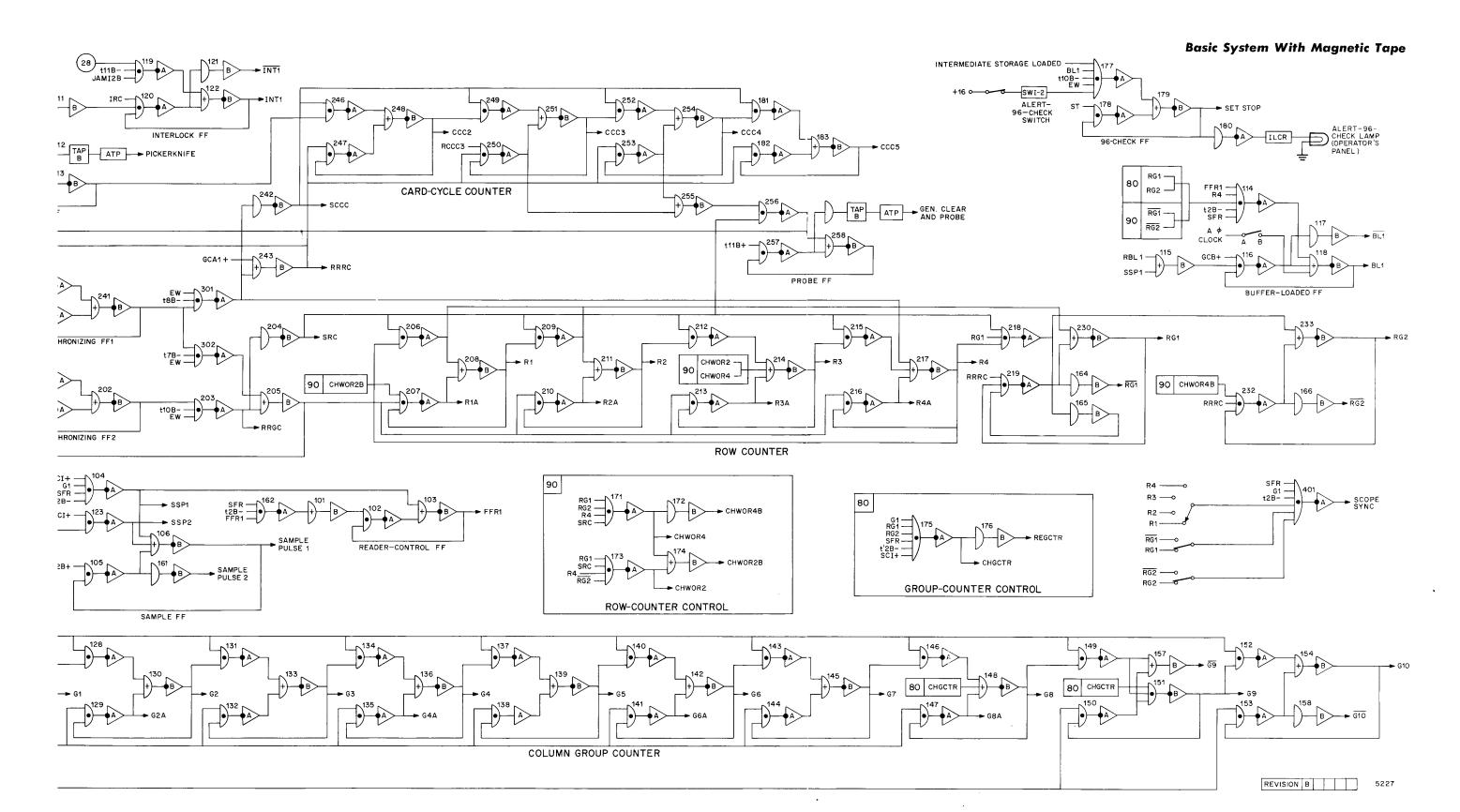
1-26A. Card-Reader Shift Register (Model 130) 1-2613

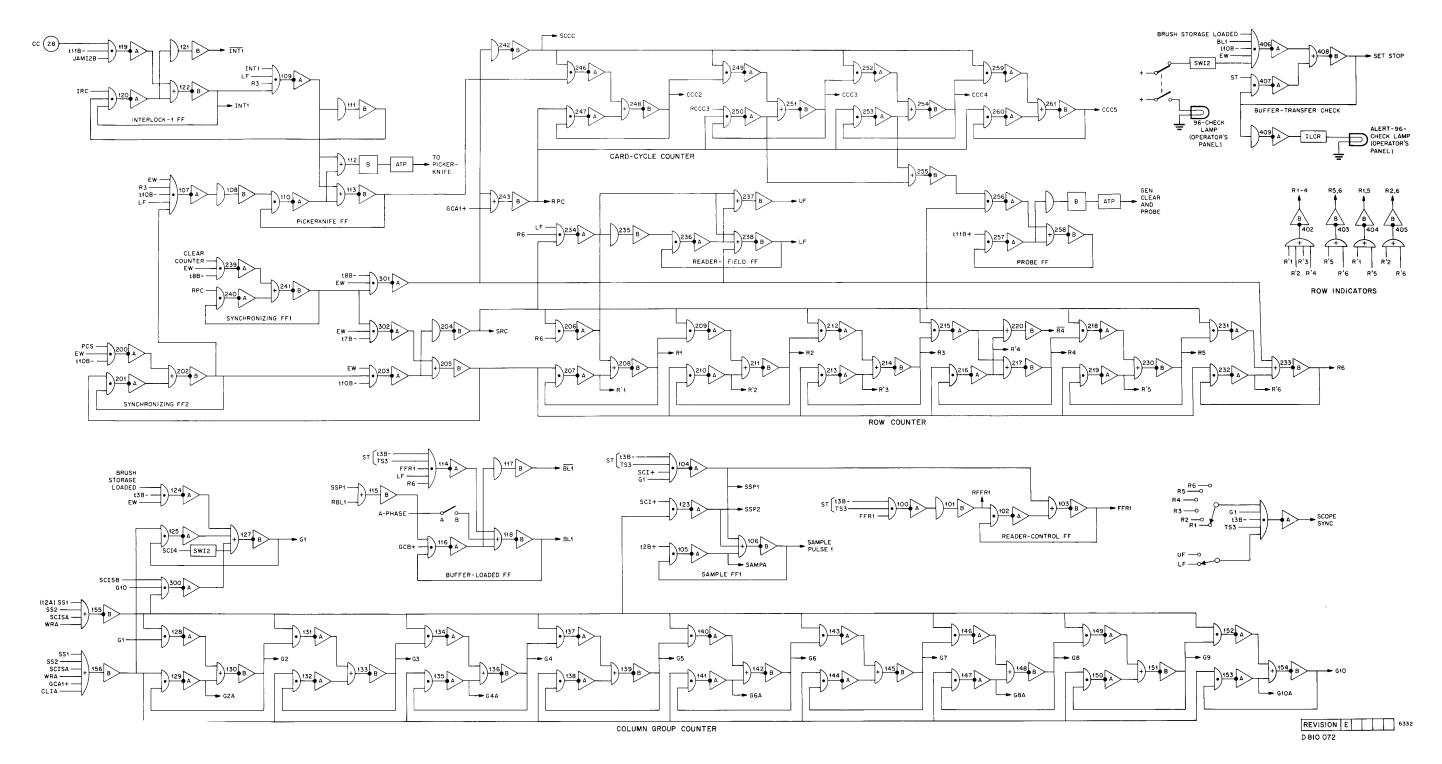


1-26A. Card-Reader Shift Register (Model 130) )-26β



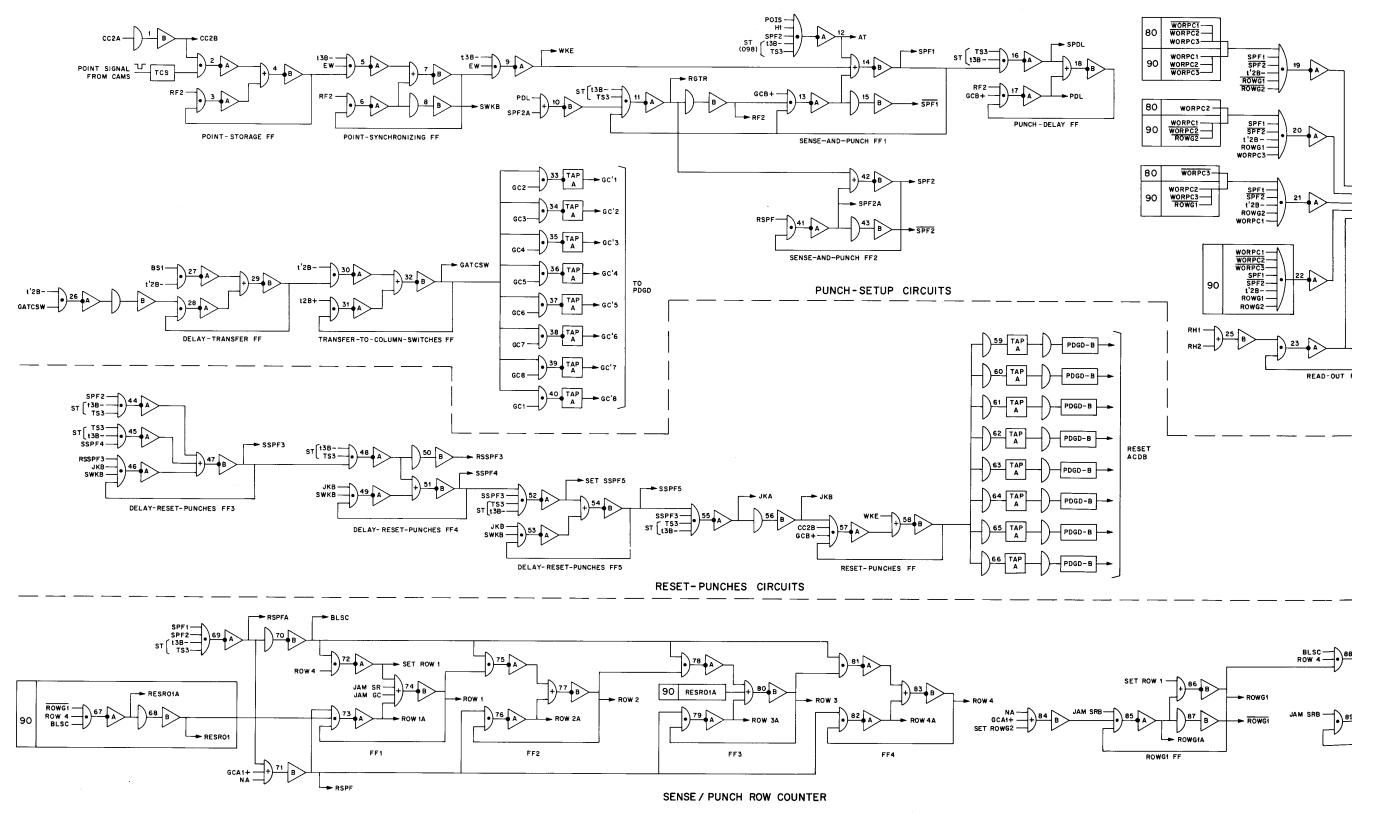
1-27A. Card-Reader Control (Model 131)



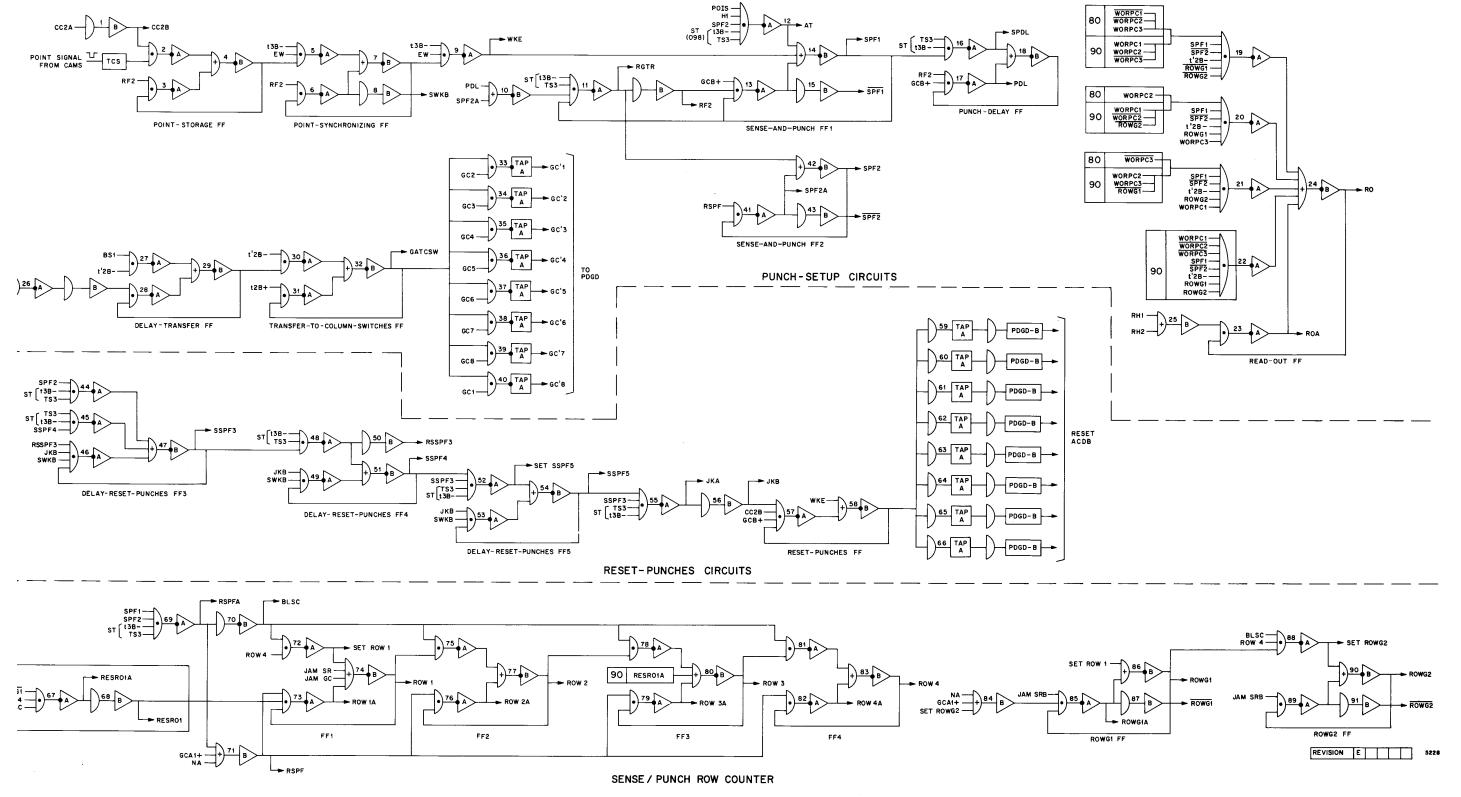


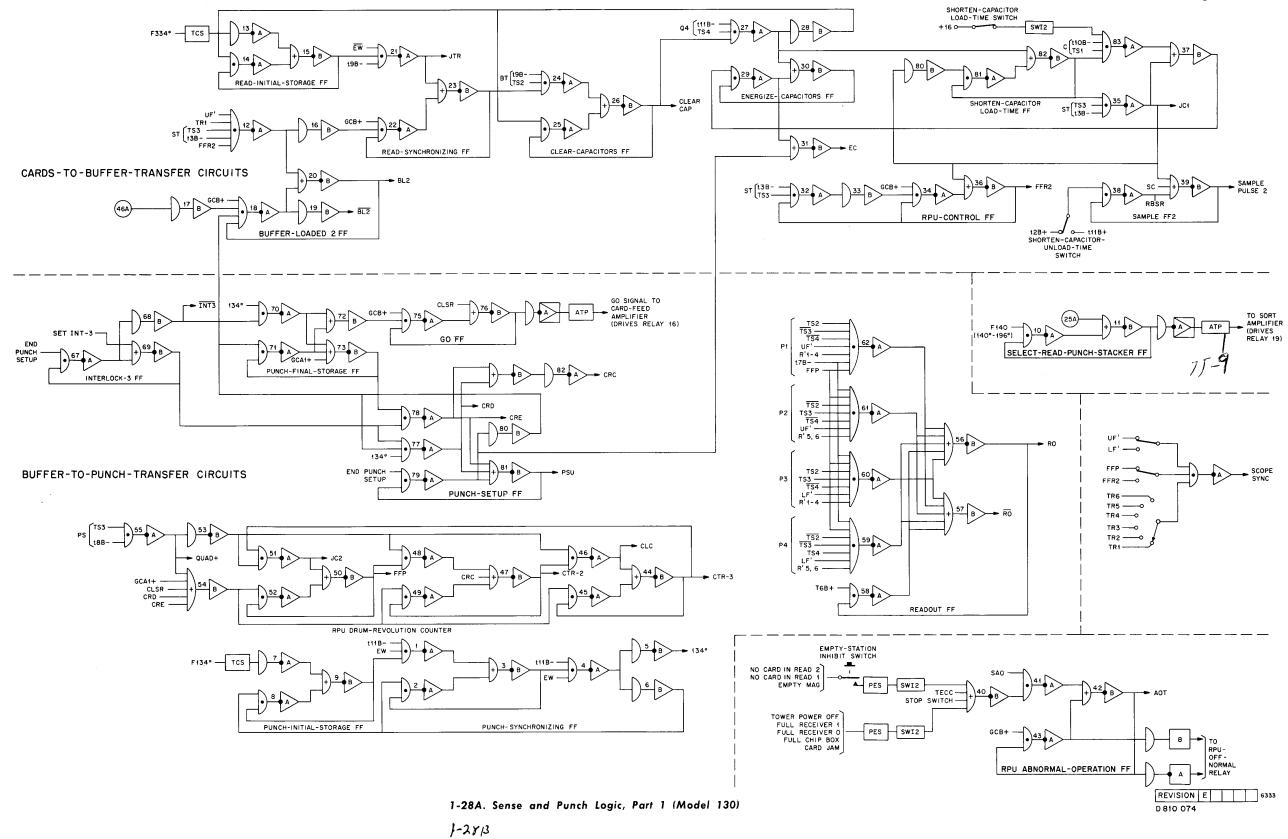
1-27A. Card-Reader Control (Model 130)

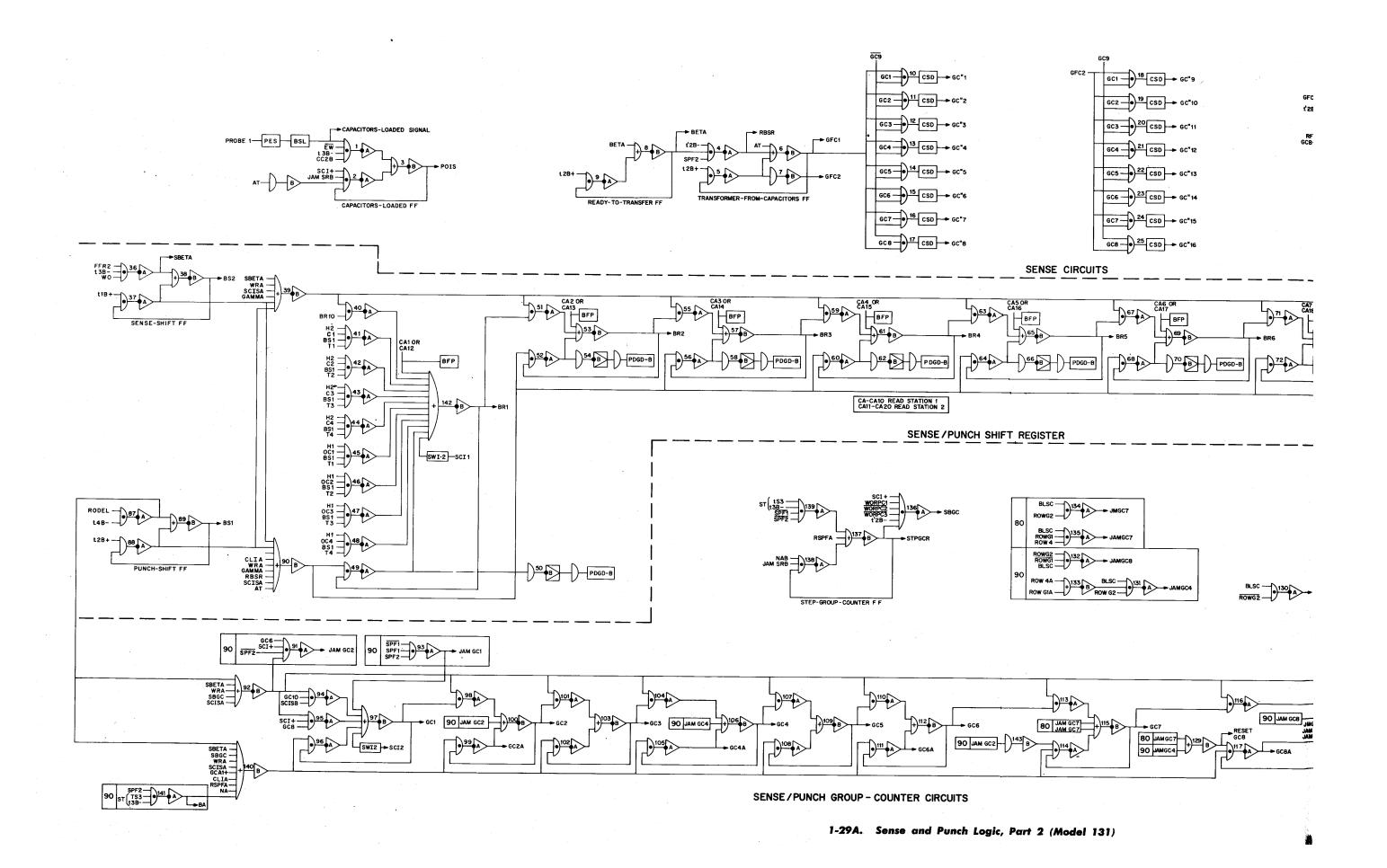
1-27B

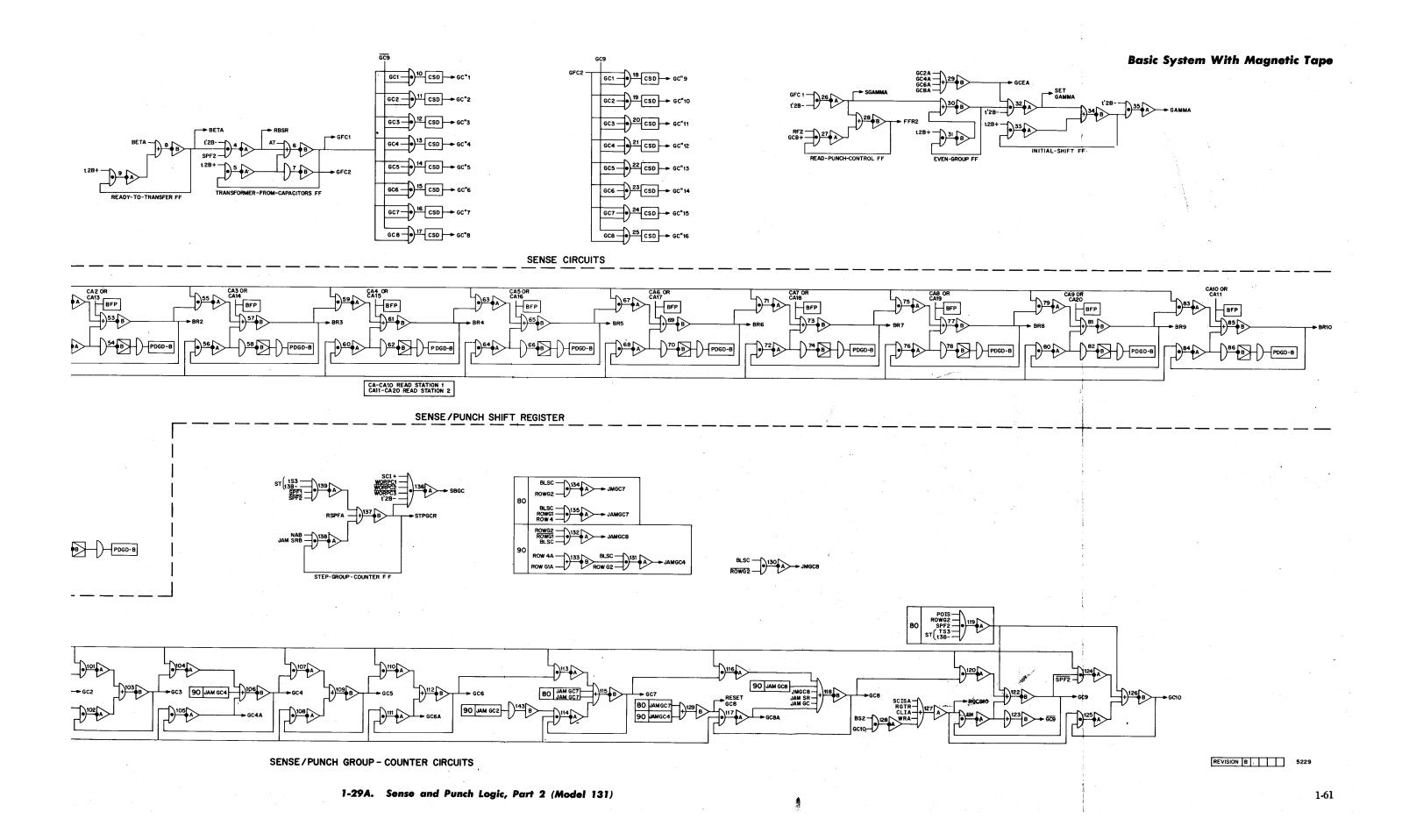


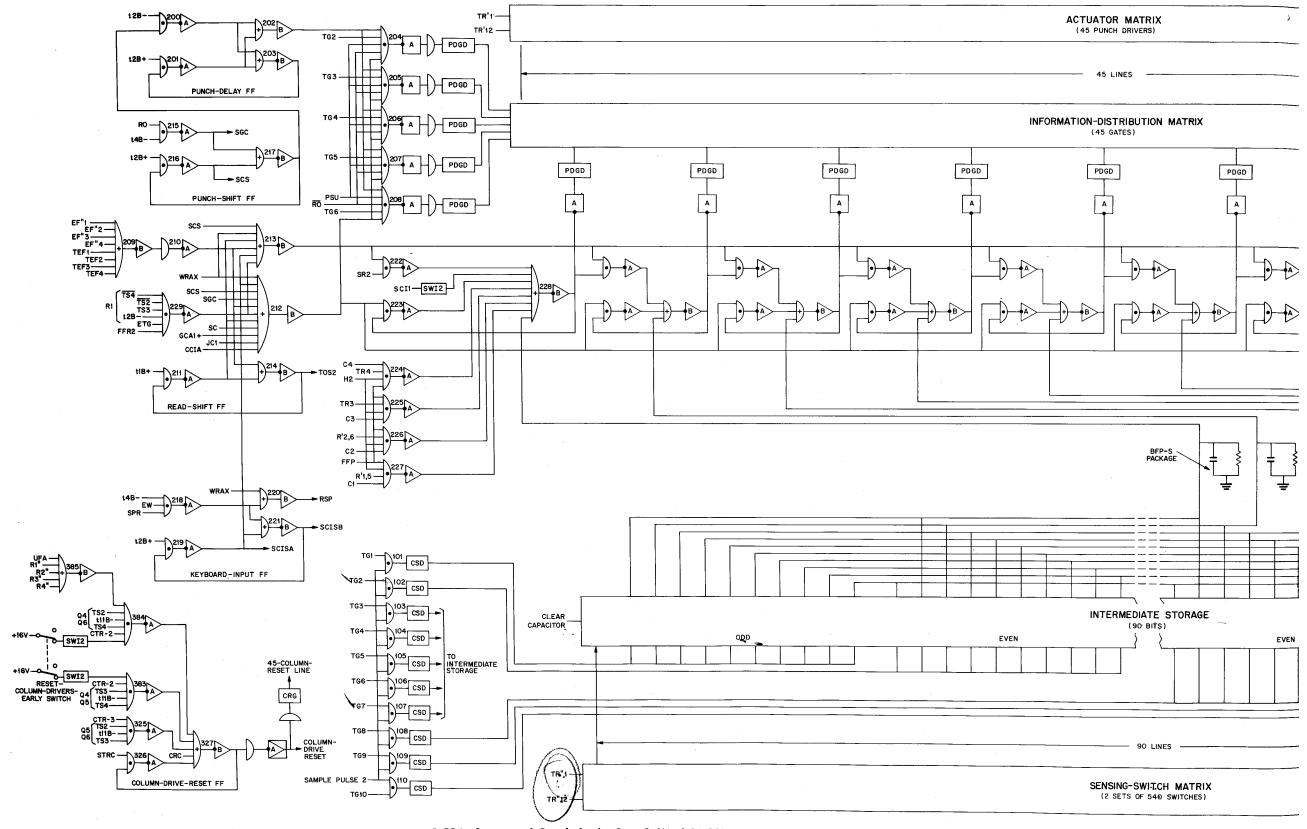
1-28A. Sense and Punch Logic, Part 1 (Model 131)











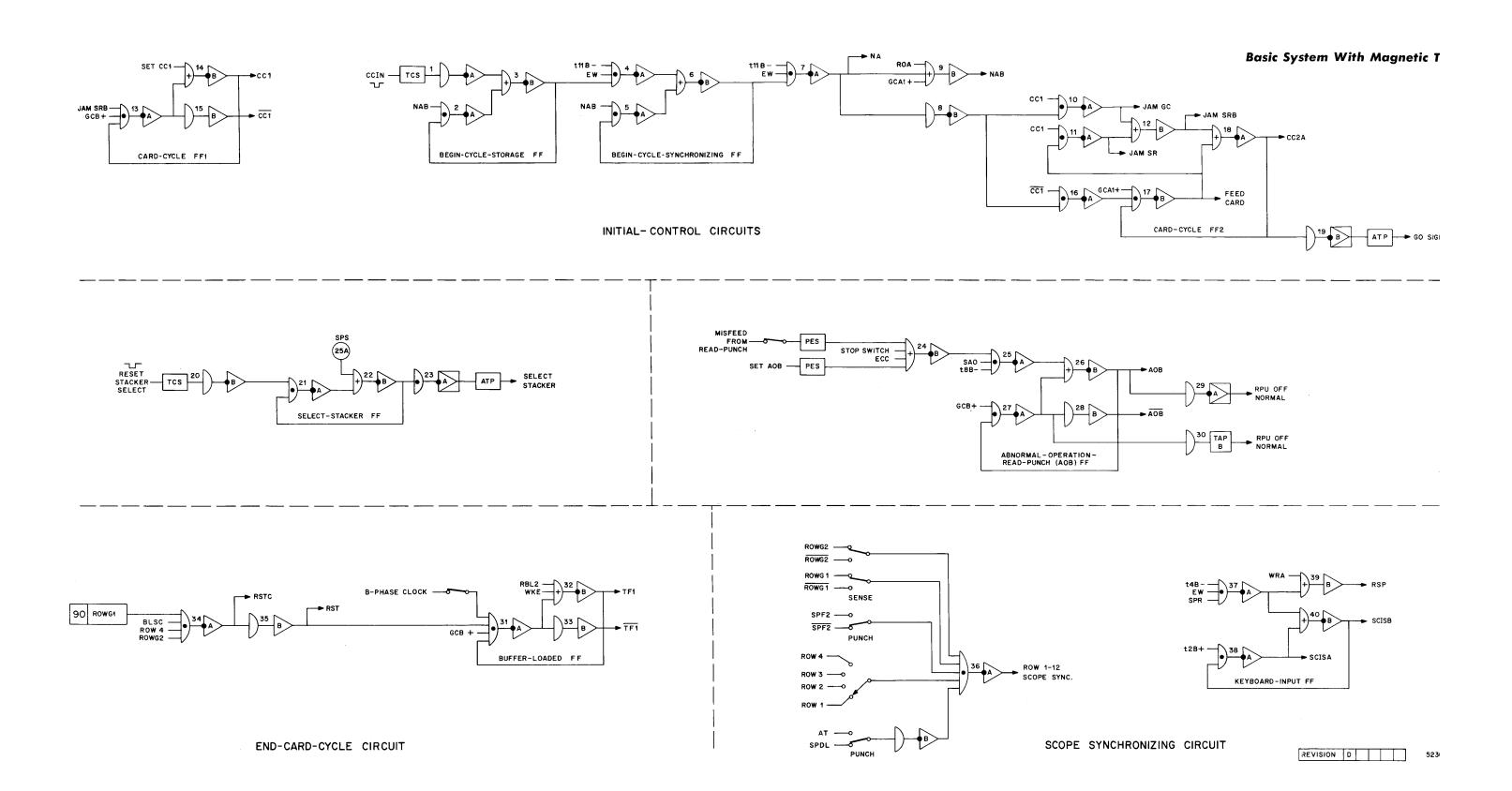
1-29A. Sense and Punch Logic, Part 2 (Model 130) /-スタル

# **Basic System With Magnetic Tape** TR'1'-ACTUATOR MATRIX (45 PUNCH DRIVERS) PDGD INFORMATION-DISTRIBUTION MATRIX (45 GATES) PDGD SCII-SWI2 ·SCISB CLEAR CAPACITOR INTERMEDIATE STORAGE (90 BITS) EVEN EVEN TR"1-PLE PULSE 2-SENSING-SWITCH MATRIX (2 SETS OF 540 SWITCHES)

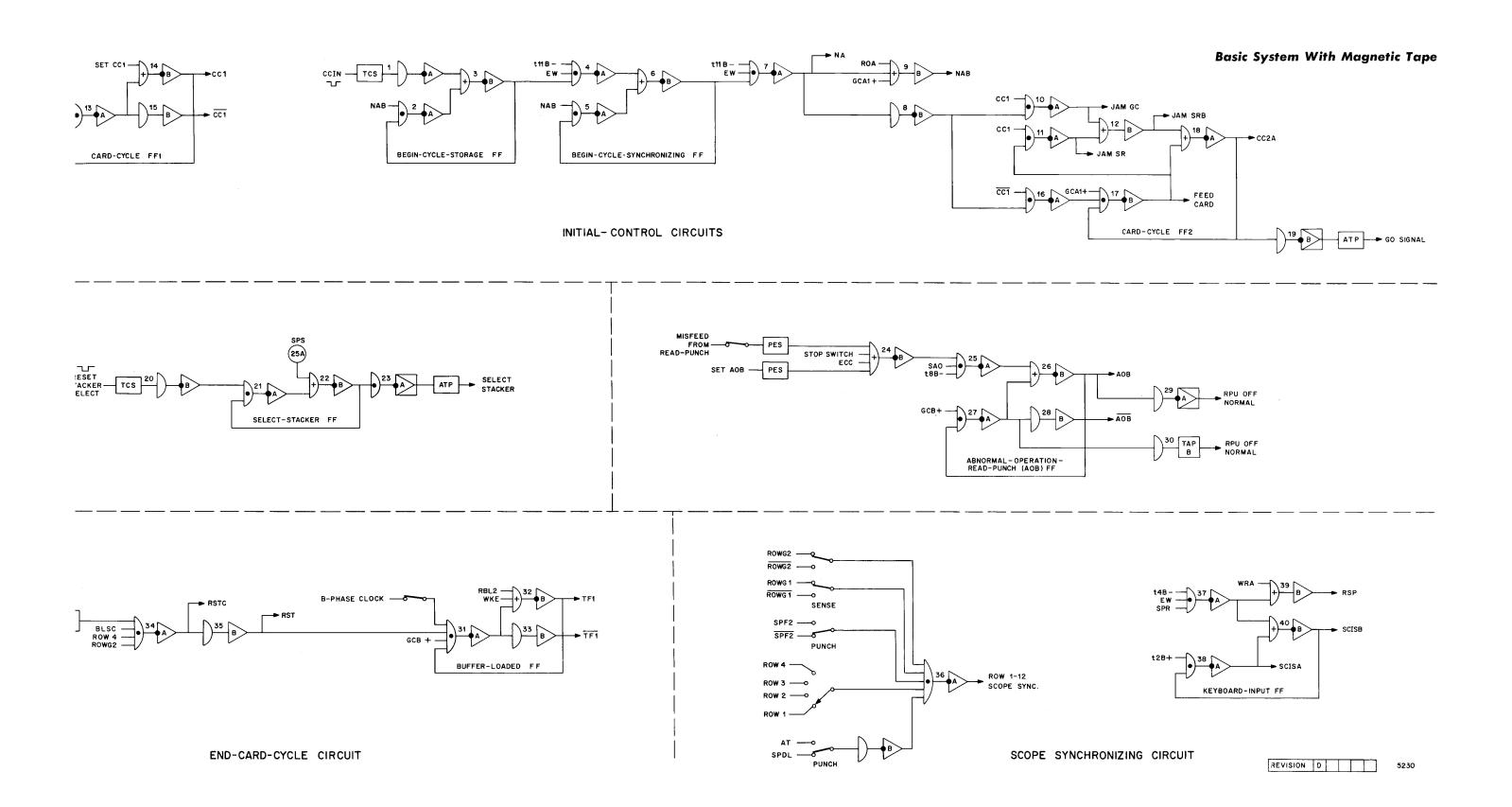
1-29A: Sense and Punch Logic, Part 2 (Model 130)

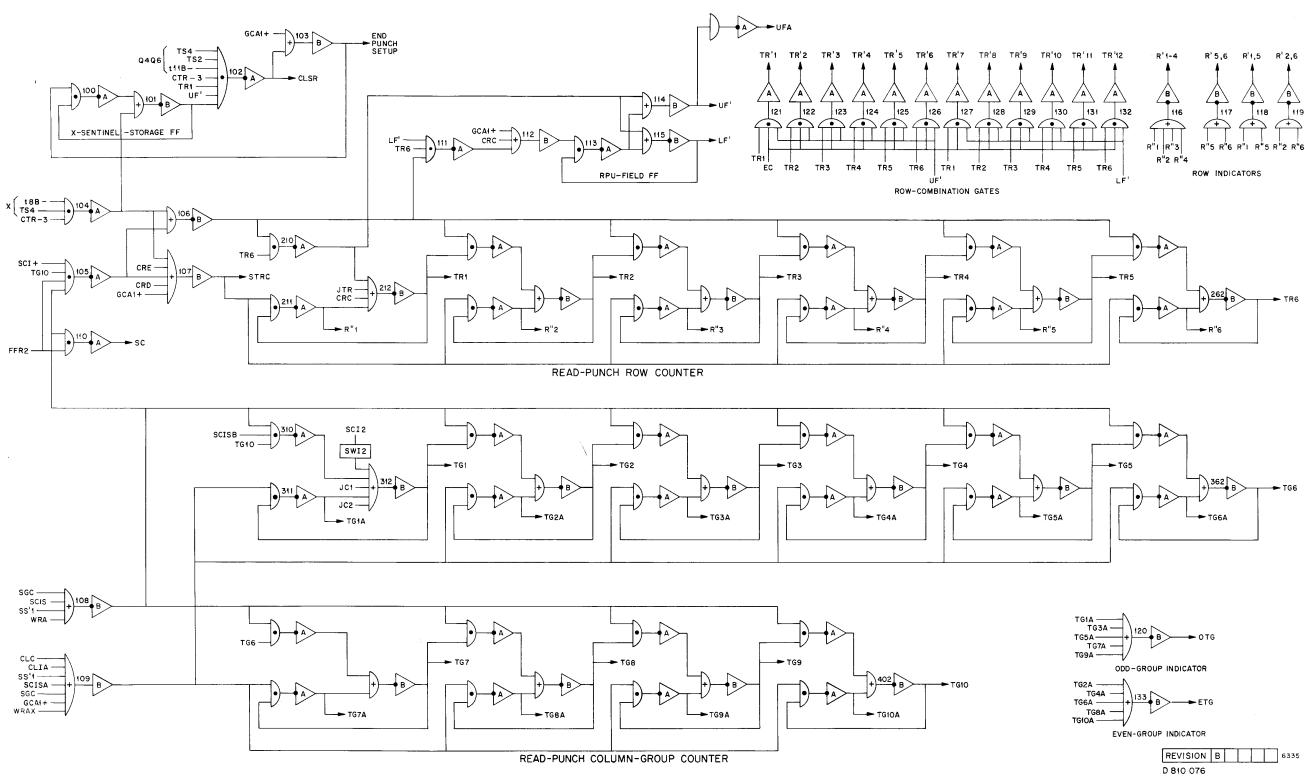
1-293

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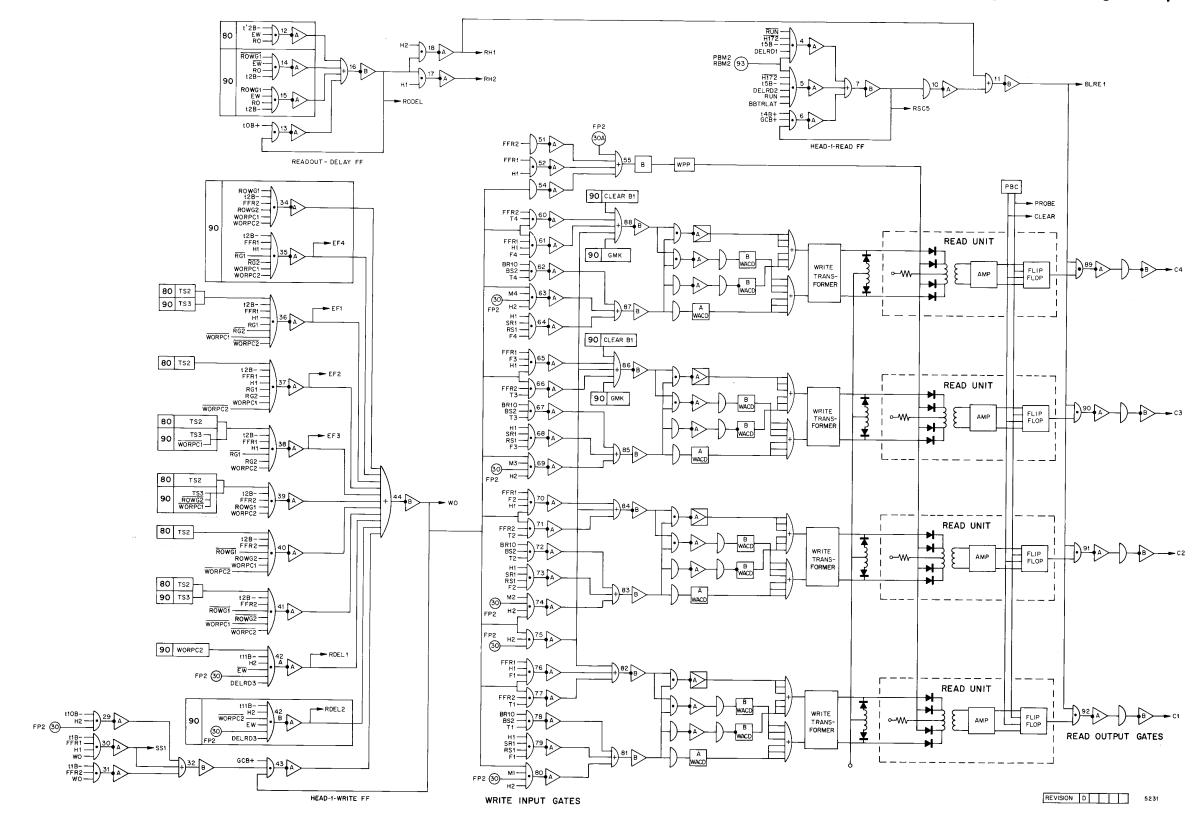
1-30A. Sense and Punch Logic, Part 3 (Model 131)

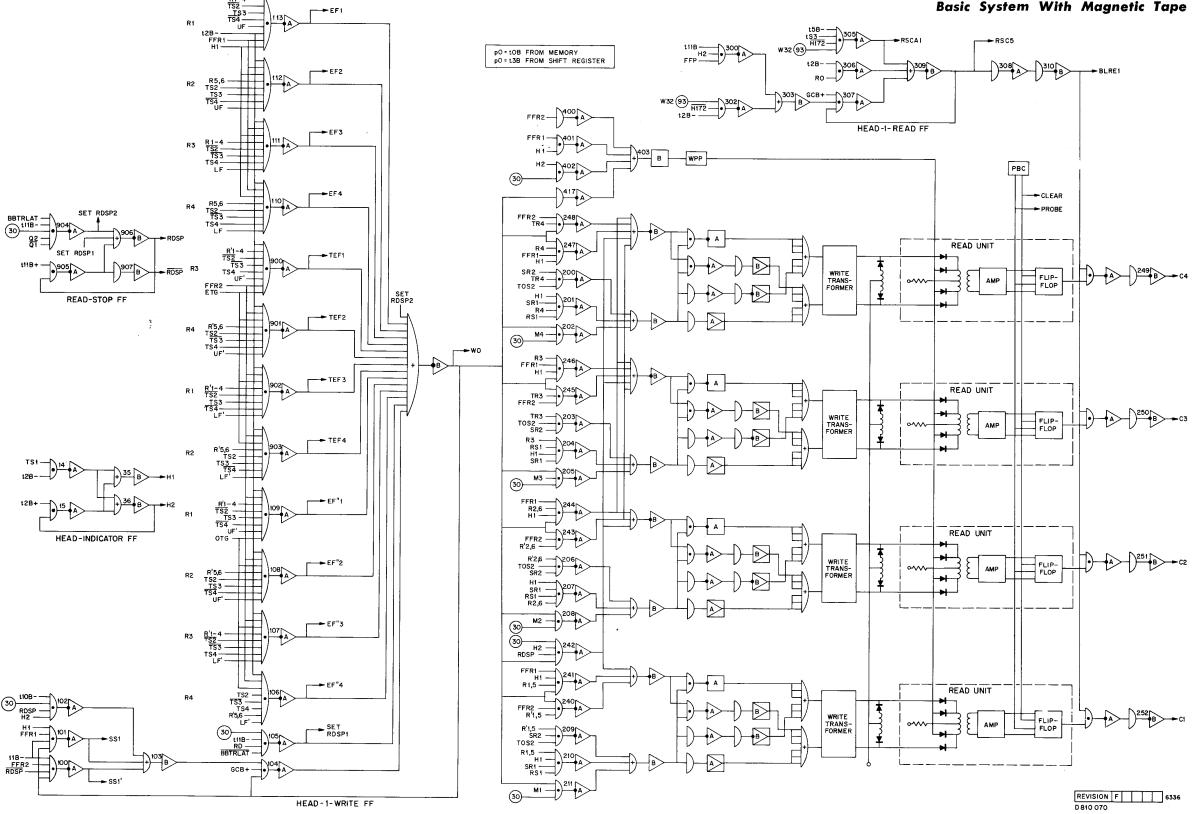




1-30A. Sense and Punch Logic, Part 3 (Model 130)

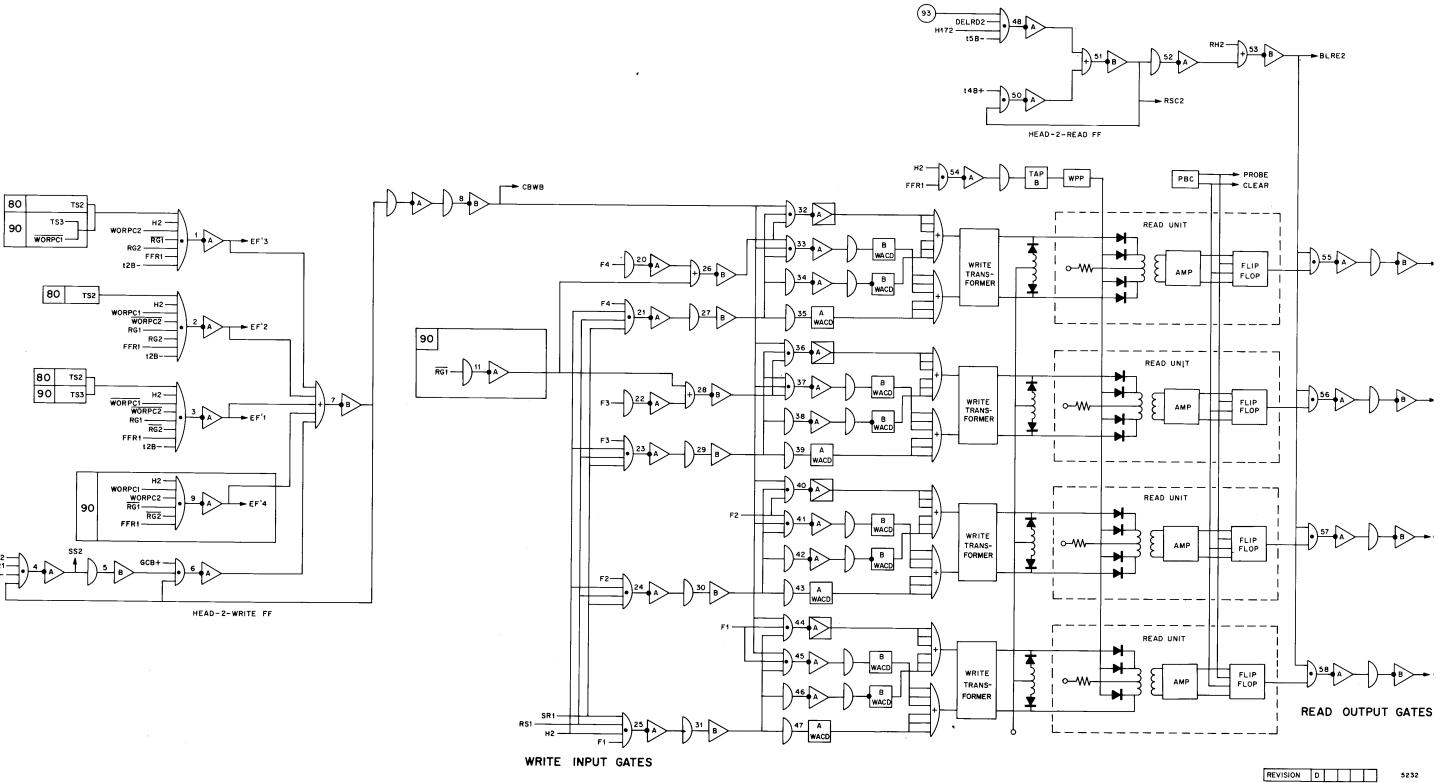
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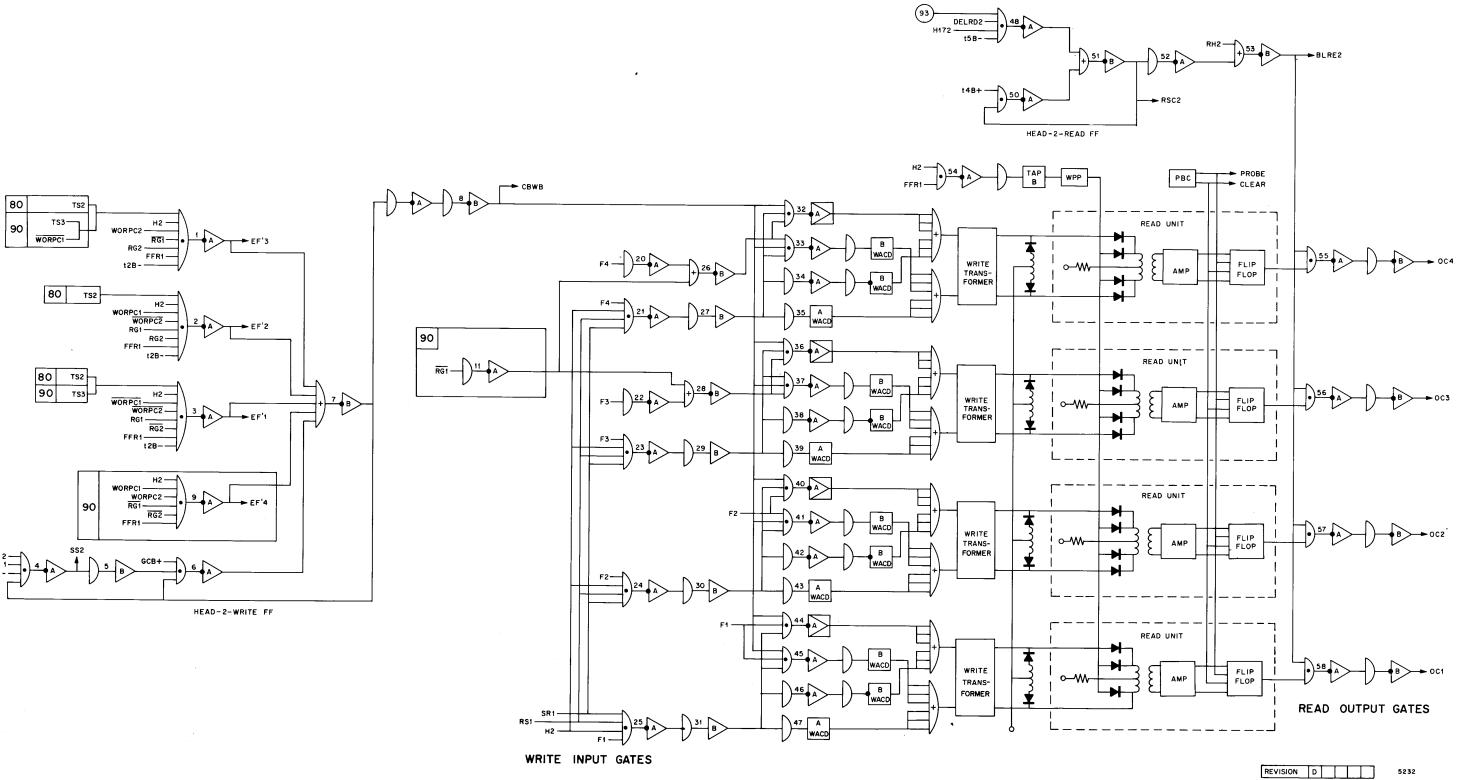


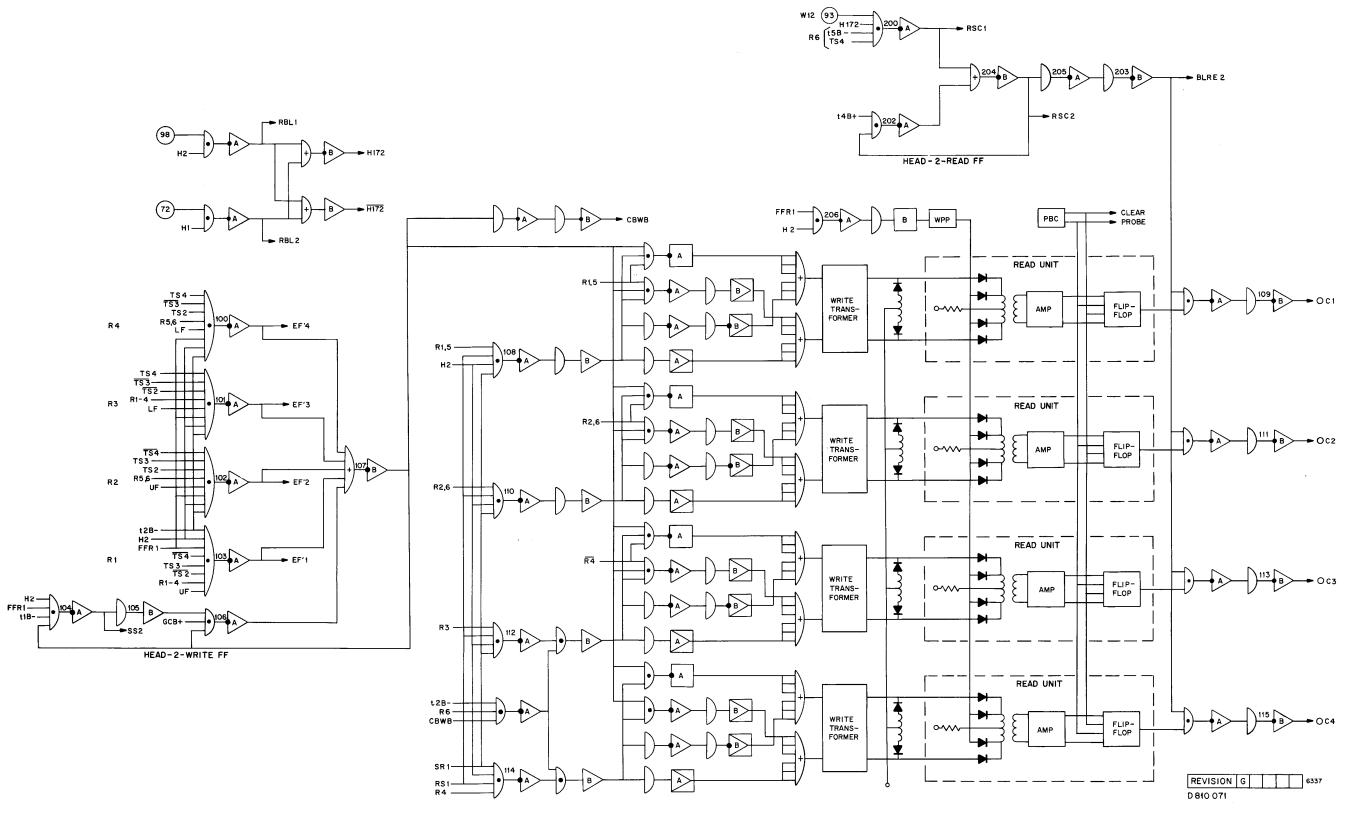


1-31A. Card-Buffer Head 1 (Model 130)

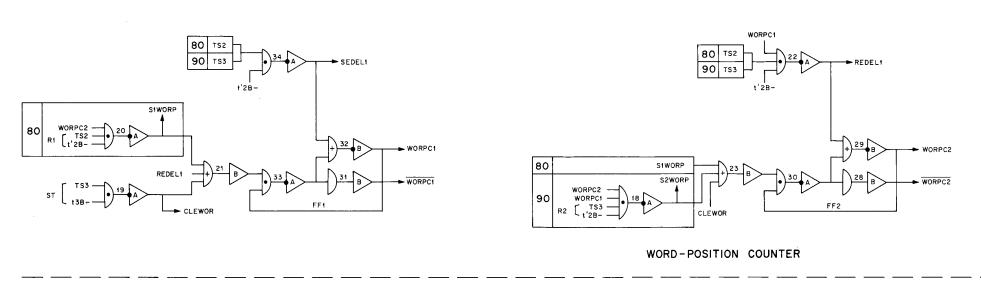
1-31B

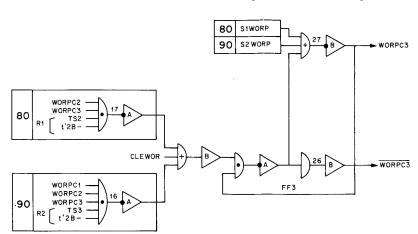


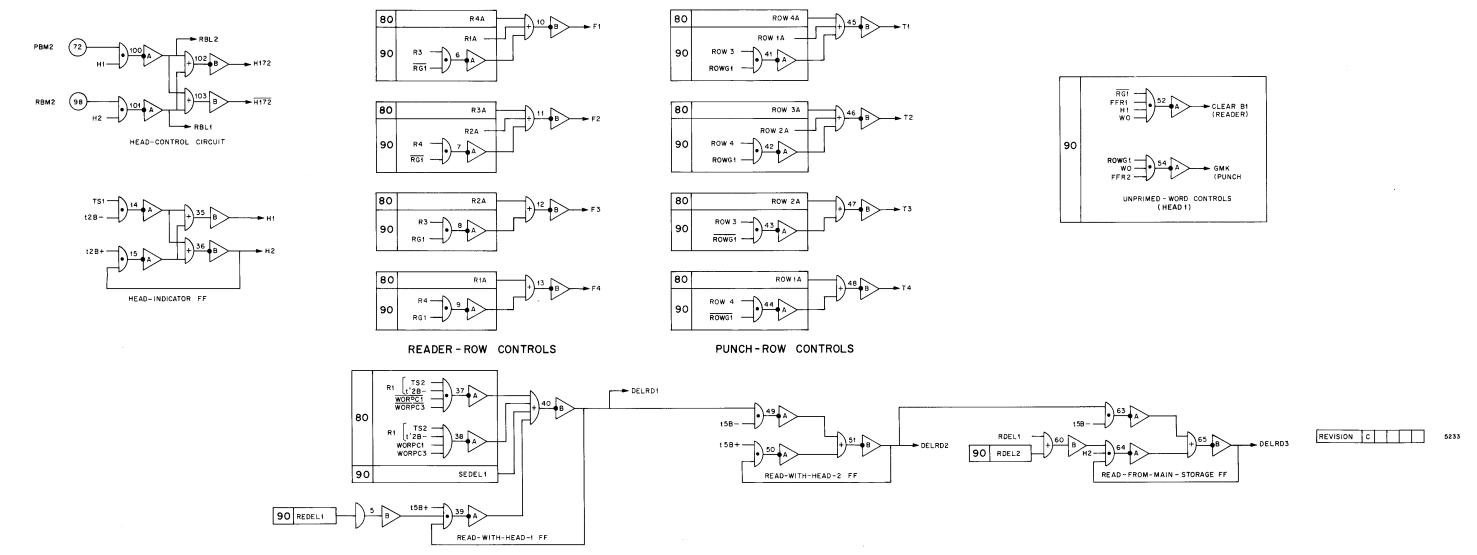




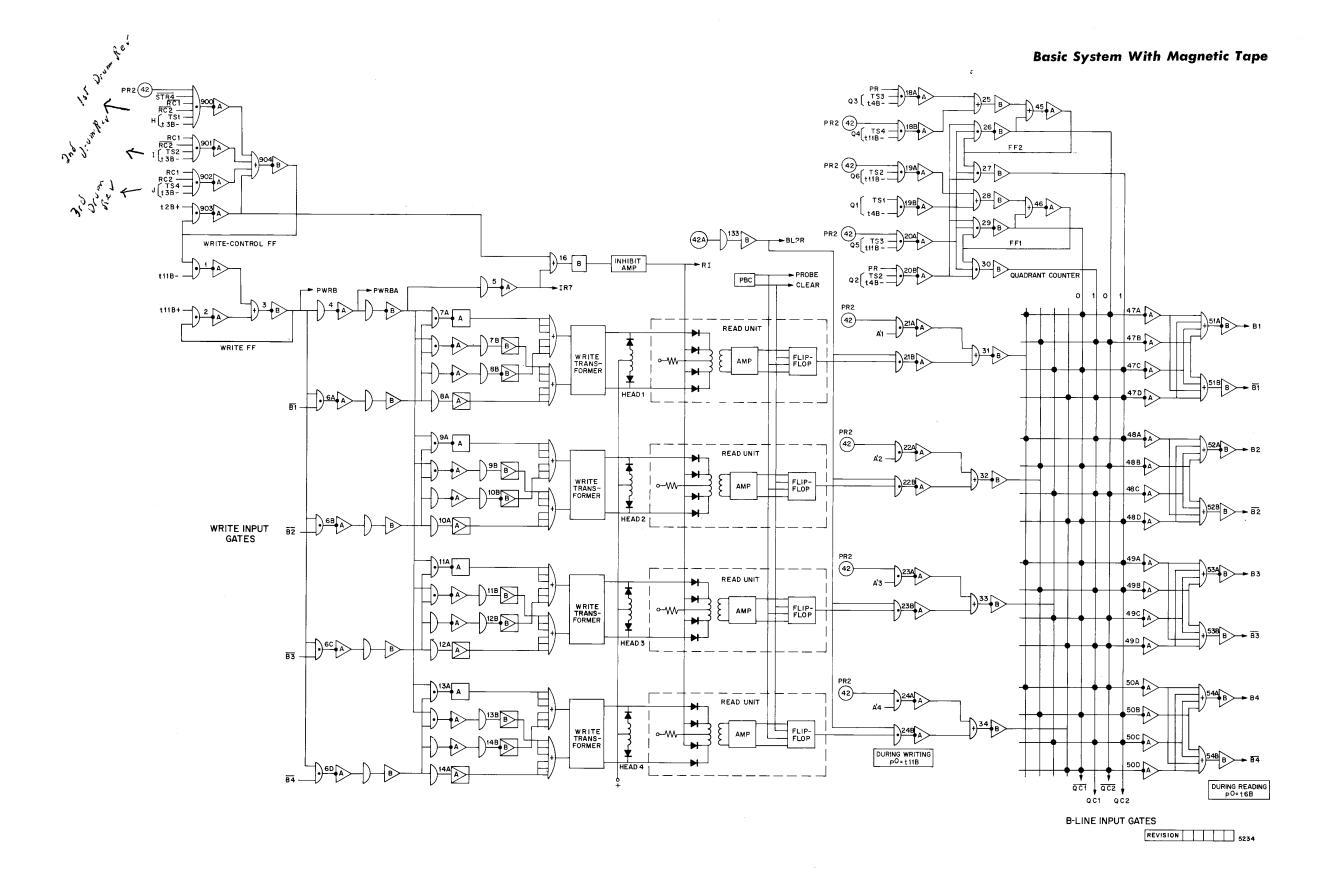
1-32A. Card-Buffer Head 2 (Model 130)

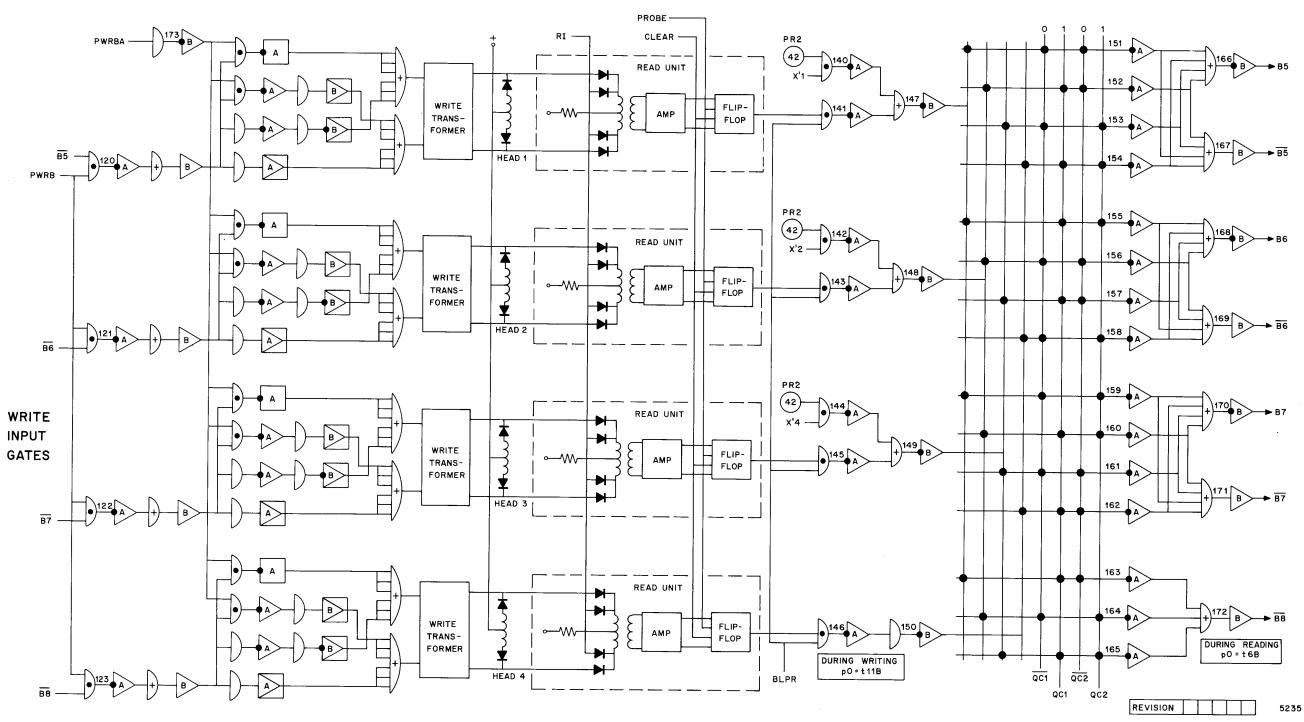




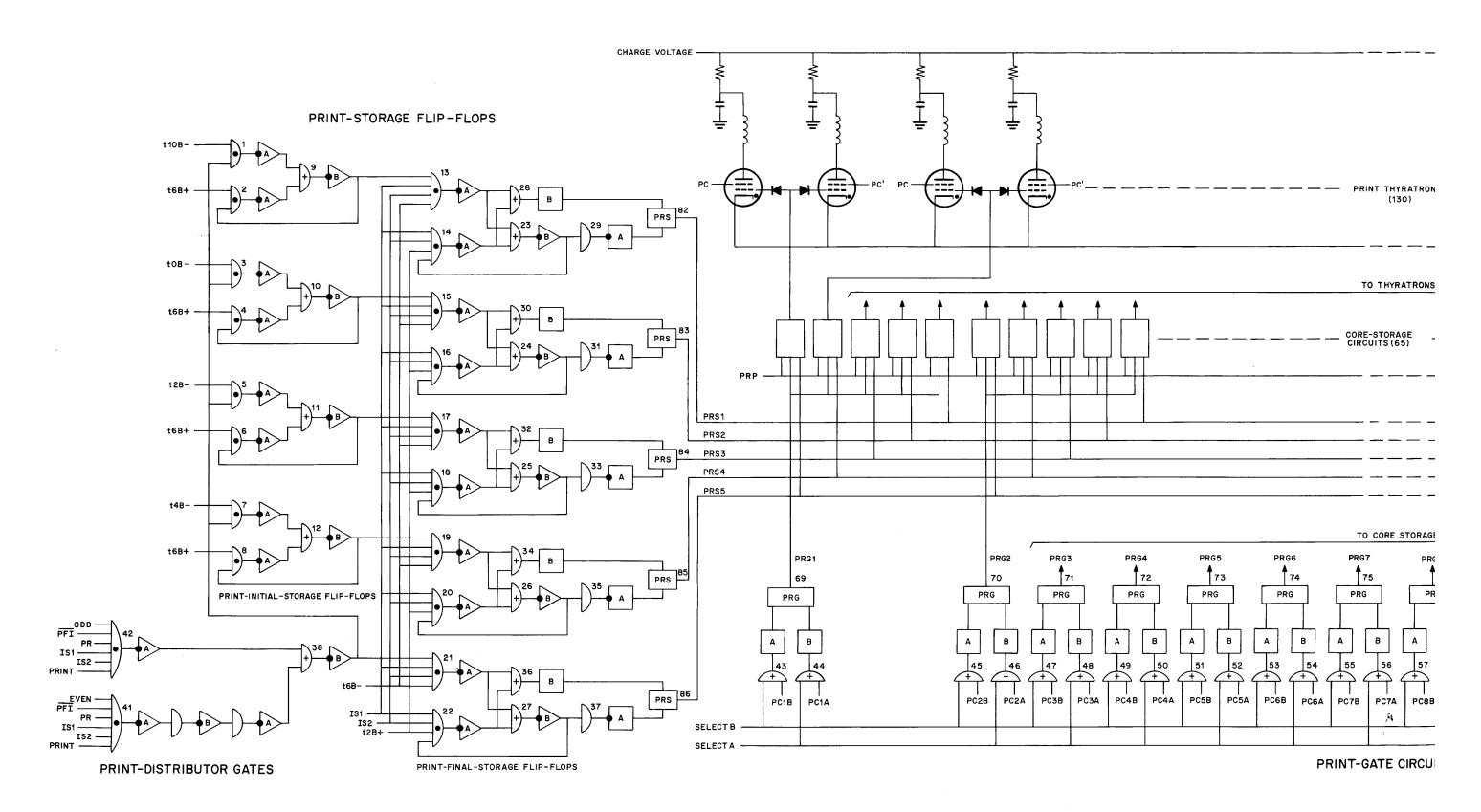


1-33A. Card-Buffer-Band Controls

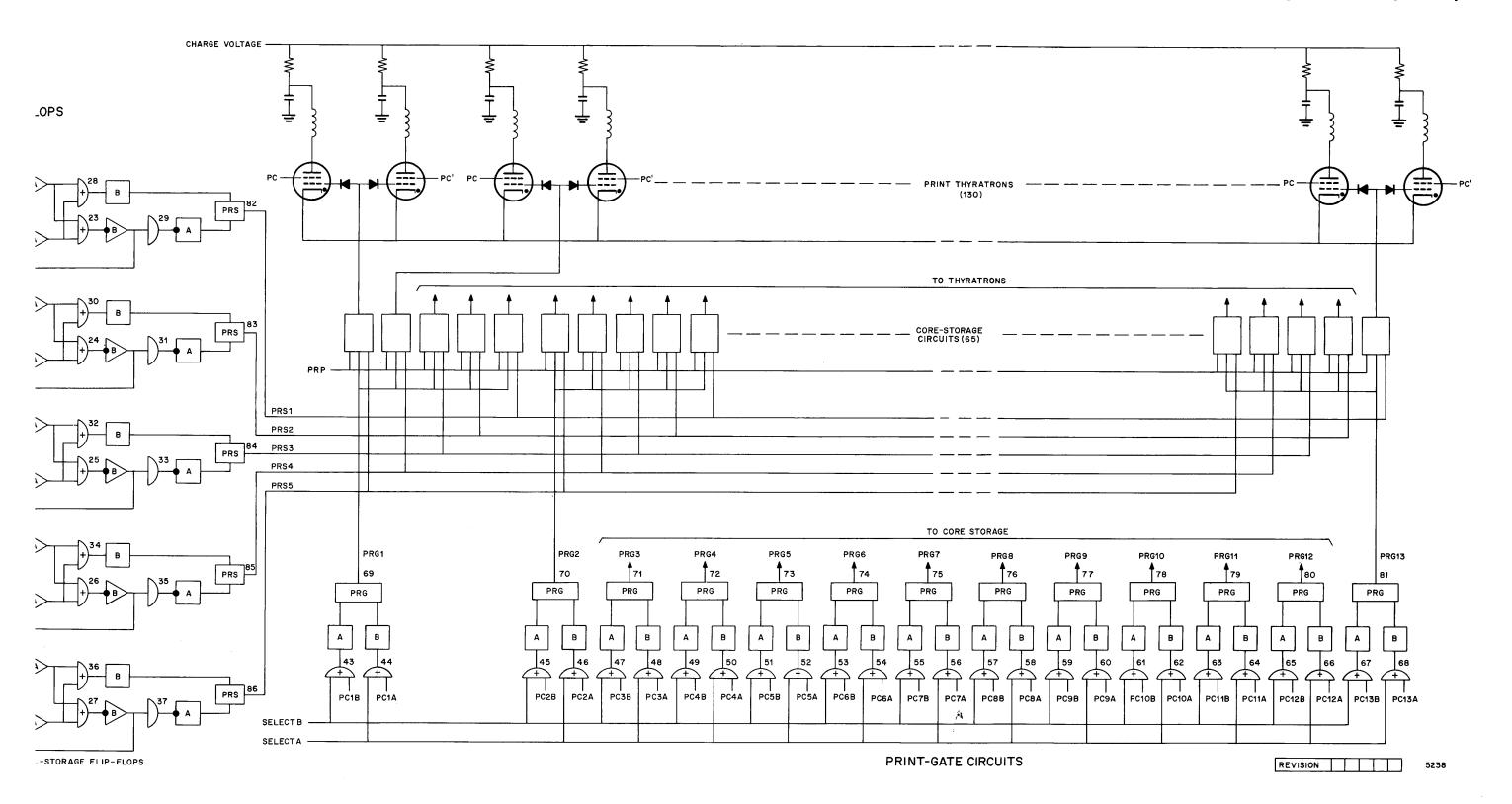


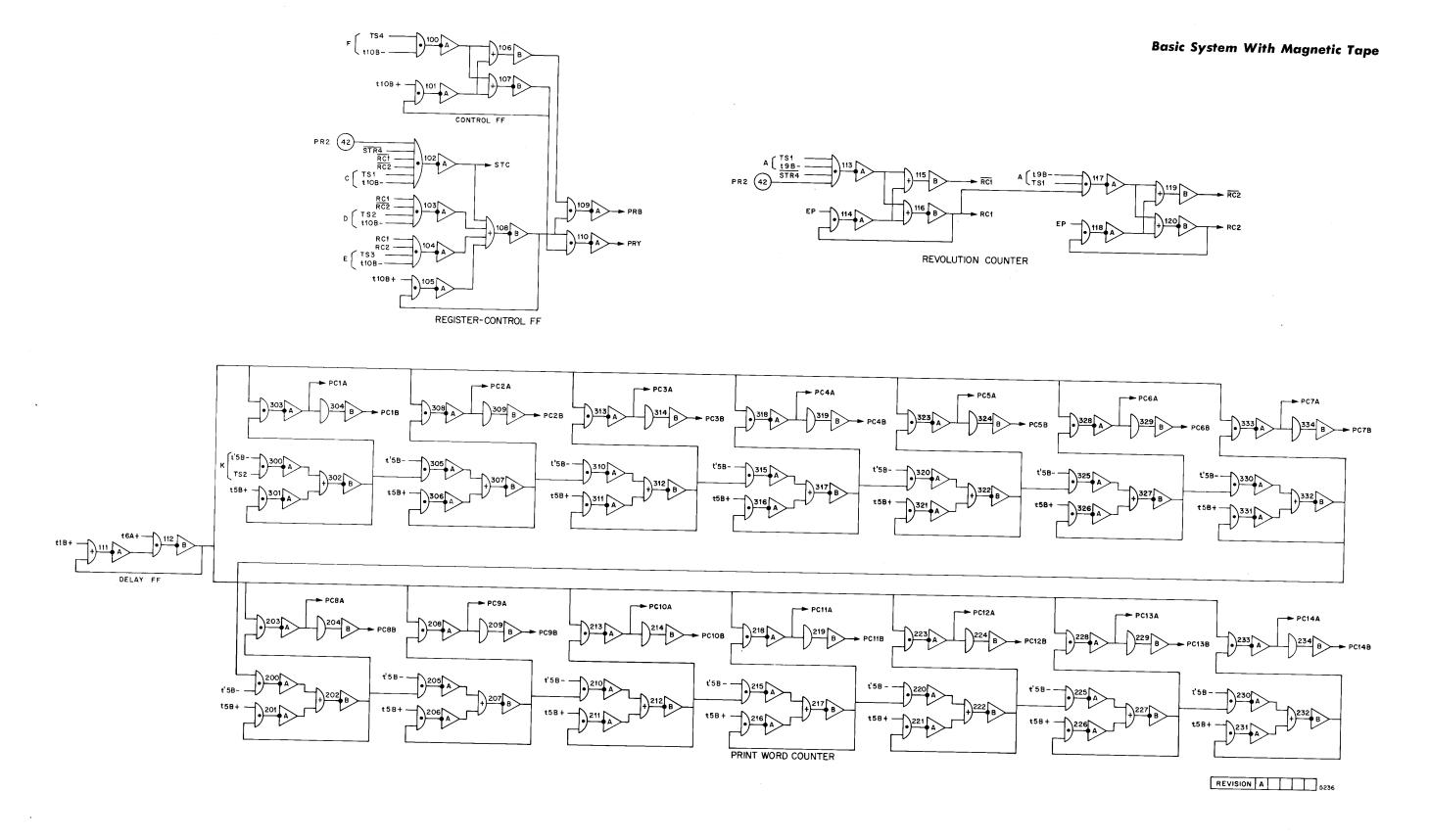


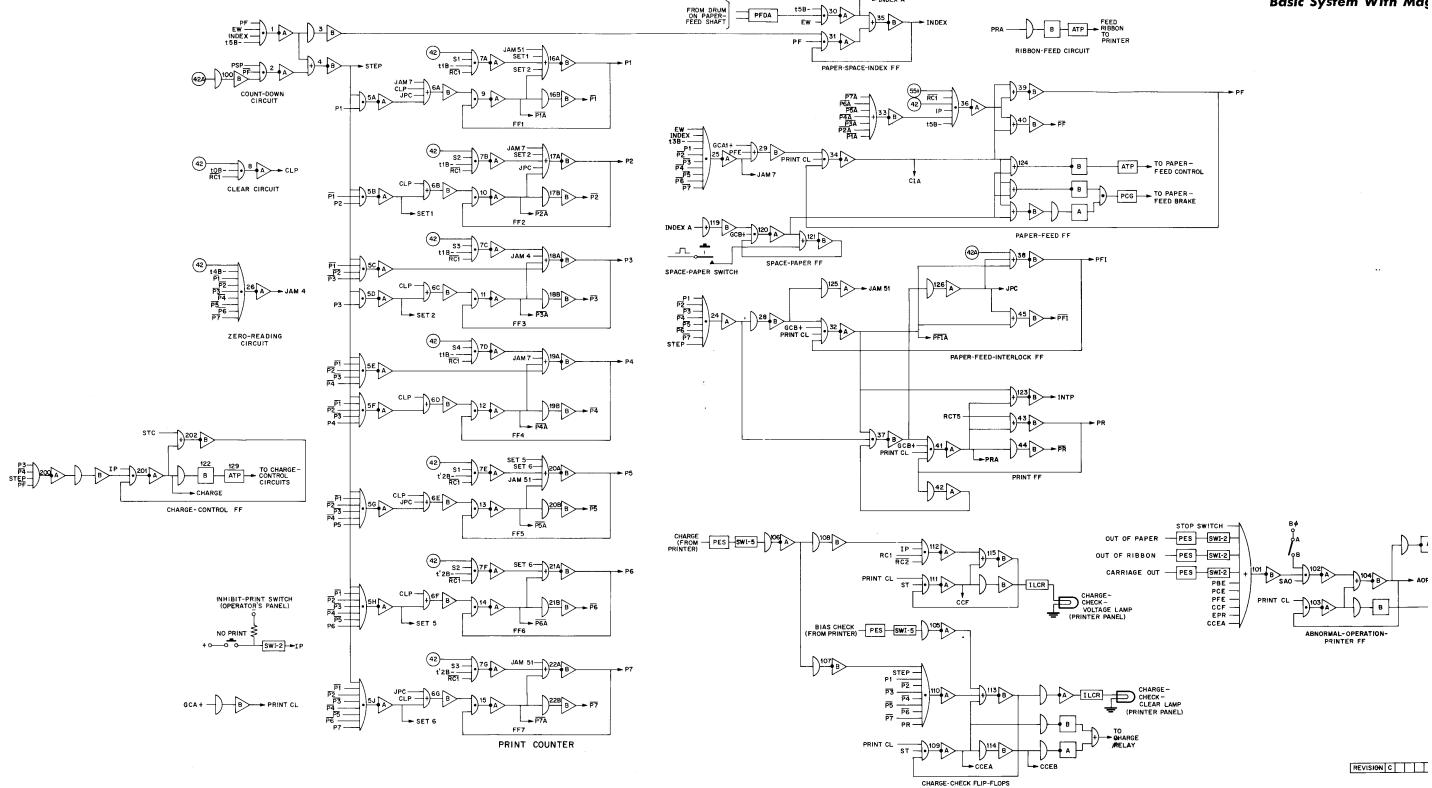
**B-LINE INPUT GATES** 



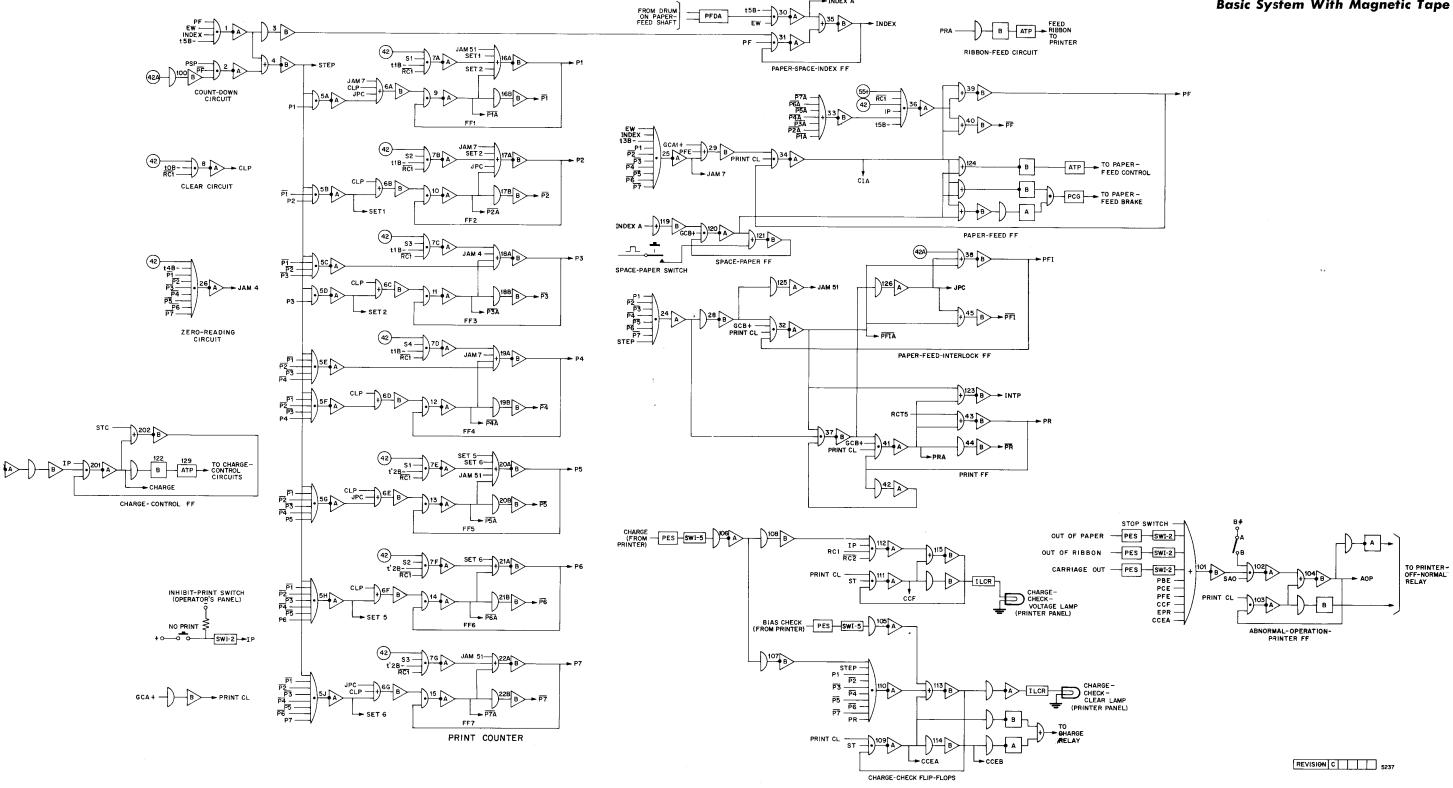
1-38A. Print Distributor







1-37A. Print Control



1-37A. Print Control 1-77

